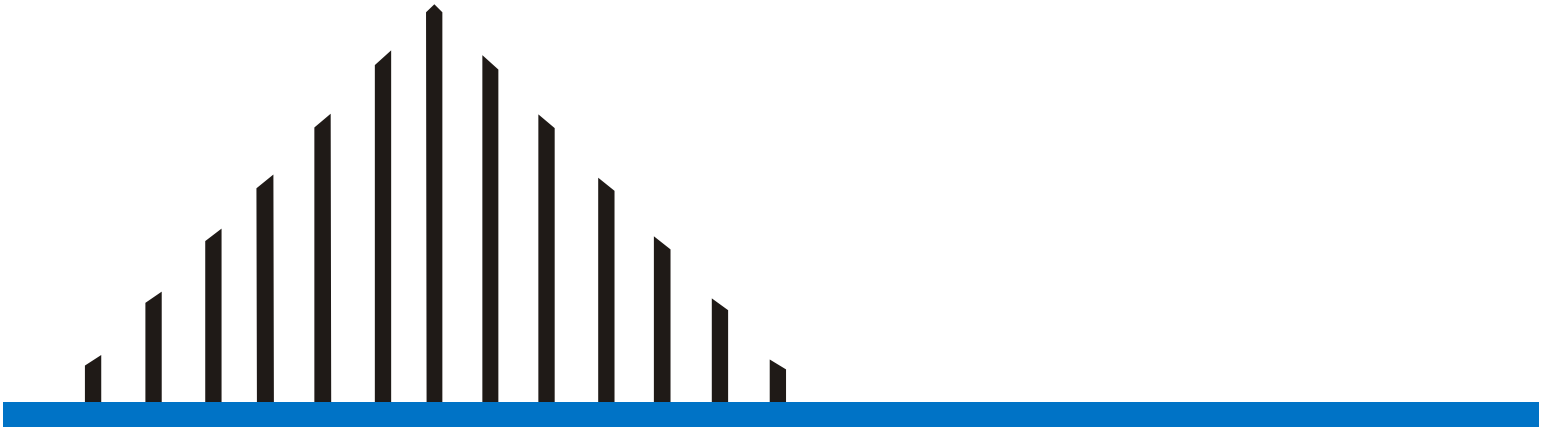
AMBE-2020™ Vocoder Chip
User's Manual

Version 4.9 February, 08



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User's Manual

Version 4.9
February, 08

Digital Voice Systems, Inc
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Data subject to change

AMBE-2020™ Vocoder Chip END USER License Agreement

1.0 Preliminary Statements and Definitions

1.1 "END USER" shall mean the person and/or organization to whom the AMBE-2020™ Vocoder Chip was delivered or provided to as specified in the purchase order or other documentation. In the event that the END USER transfers his rights under this license to a third party as specified in section 2.2, then this third party shall become an "END USER".
1.2 Digital Voice Systems, Inc. (DVSI) has developed a voice coding method and algorithm (the "Technology") based on the Advanced Multi-Band Excitation ("AMBE®") voice coder. The technology codes speech at bit rates of 2.4 to 9.6 kilobits per second (kbps) including error correction bits.
1.3 "AMBE® Voice Compression Software" shall mean the speech coding software and/or firmware integrated into the AMBE-2020™ Vocoder chip integrated circuit.
1.4 "Voice Codec" shall mean the AMBE-2020™ Vocoder Chip integrated circuit, the AMBE® Voice Compression Software, firmware and associated documentation, including modifications, enhancements and extensions made by or for Digital Voice Systems, Inc. (DVSI) and including circuit diagrams, timing diagrams, logic diagrams, layouts, operating instructions and user manuals.
1.5 DVSI represents that it owns certain "Proprietary Rights" in the Technology and the AMBE® Voice Compression Software, including patent rights in the Technology, and patent rights, copyrights, and trade secrets in the AMBE® Voice Compression Software.

2.0 License Granted

2.1 Subject to the conditions herein and upon initial use of the AMBE-2020™ Vocoder Chip, DVSI hereby grants to END USER a non-exclusive, limited license to use the AMBE® Voice Compression Software in machine readable form solely on the AMBE-2020™ Vocoder Chip. Title to the AMBE® Voice Compression Software remains with DVSI. No license is granted for use of the AMBE® Voice Compression Software on other than the AMBE-2020™ Vocoder Chip. No license, right or interest in any trademark, trade name or service mark of DVSI is granted under this Agreement.
2.2 END USER shall not copy, extract, de-compile, reverse engineer or disassemble the AMBE® Voice Compression Software contained in the AMBE-2020™ Vocoder Chip.

3.0 Transfer of License

3.1 The END USER shall have the right to transfer the AMBE-2020™ Vocoder Chip and all rights under this Agreement to a third party by either (i) providing the third party with a copy of this Agreement or (ii) providing the third party with an agreement written by the END USER (hereinafter "END USER Agreement") so long as the END USER Agreement is approved in writing by DVSI prior to transfer of the AMBE-2020™ Vocoder Chip. The END USER Agreement shall contain comparable provisions to those contained herein for protecting the Proprietary Information from disclosure by such third party. Third parties shall agree to accept all the terms and conditions under either Agreement or the END USER Agreement.

4.0 Term and Termination

4.1 This Agreement is effective upon initial delivery of the Voice Codec and shall remain in effect until terminated in accordance with this agreement.
4.2 This Agreement shall terminate automatically without notice from DVSI if END USER fails to comply with any of the material terms and conditions herein. END USER may terminate this Agreement at any time upon written notice to DVSI certifying that END USER has complied with the provisions of Section 3.3.
4.3 Upon termination of this Agreement for any reason, END USER shall: (i) return all AMBE-2020™ Vocoder Chip purchased or acquired, or in Licensee's possession, to DVSI; (ii) have no further rights to any AMBE® Voice Compression Software or the Technology without a separate written license from DVSI; (iii) discontinue all use of the AMBE-2020™ Vocoder Chip;

5.0 Payments

5.1 In consideration of the materials provided as part of the Voice Codec, and in consideration of the license and rights in the AMBE® Voice Compression Software granted by DVSI, and in consideration of DVSI's performance of its obligations hereunder, END USER agrees to pay to DVSI the fee specified in DVSI's invoice.

6.0 Proprietary Notices

6.1 END USER shall not remove any copyright or proprietary notice on the AMBE-2020™ Vocoder Chip or on the AMBE® Voice Compression Software.

7.0 Proprietary Information

7.1 The parties agree that the AMBE® Voice Compression Software shall be considered Proprietary Information.
7.2 Except as otherwise provided in this Agreement, END USER shall not use, disclose, make, or have made any copies of the Proprietary Information, in whole or in part, without the prior written consent of DVSI.

8.0 Limited Warranty

8.1 DVSI warrants the Voice Codec to be free from defects in materials and workmanship under normal use for a period of ninety (90) days from the date of delivery.
8.2 Except as stated in Section 7.1, the Voice Codec is provided "as is" without warranty of any kind. DVSI does not warrant, guarantee or make any representations regarding the use, or the results of the use, of the Voice Codec with respect to its correctness, accuracy, reliability, correctness or otherwise. The entire risk as to the results and performance of the Voice Codec is assumed by the END USER. After expiration of the warranty period, END USER, and not DVSI or its employees, assumes the entire cost of any servicing, repair, replacement, or correction of the Voice Codec.
8.3 DVSI represents that, to the best of its knowledge, it has the right to enter into this Agreement and to grant a license to use the AMBE® Voice Compression Software to END USER.
8.4 Except as specifically set forth in this Section 7.0, DVSI makes no express or implied warranties including, without limitation, the warranties of merchantability or fitness for a particular purpose or arising from a course of dealing, usage or trade practice, with respect to the Voice Codec. Some states do not allow the exclusion of implied warranties, so the above exclusion may not apply to END USER. No oral or written information or advice given by DVSI or its employees shall create a warranty or in any way increase the scope of this warranty, and END USER may not rely on any such information or advice. The limited warranties under this section 7.0 give END USER specific legal rights, and END USER may have other rights which vary from state to state.

9.0 Limitation of Liability

9.1 In no event shall DVSI be liable for any special, incidental, indirect or consequential damages resulting from the use or performance of the Voice Codec whether based on an action in contract, tort (including negligence) or otherwise (including, without limitation, damages for loss of business profits, business interruption, and loss of business information), even if DVSI or any DVSI representative has been advised of the possibility of such damages.
9.2 Because some states do not allow the exclusion or limitation of liability for consequential or incidental damages, the above limitations may not apply to END USER.
9.3 DVSI's maximum liability for damages arising under this Agreement shall be limited to 20% (twenty percent) of the fees paid by END USER for the particular Voice Codec which caused the damages or that is the subject matter of, or is directly related to, the cause of action.

10.0 Taxes

10.1 All payments required under Section 4.0 or otherwise under this Agreement are exclusive of taxes and END USER agrees to bear and be responsible for the payment of all such taxes (except for taxes based upon DVSI's income) including, but not limited to, all sales, use, rental receipt, personal property or other taxes which may be levied or assessed in connection with this Agreement.

11.0 Export

11.1 United States export laws and regulations prohibit the exportation of certain products or technical data received from DVSI under this Agreement to certain countries except under a special validated license. As of November 30, 1999 the restricted countries are: Libya, Cuba, North Korea, Iraq, Serbia, Taliban in Afghanistan, Sudan, Burma, Yugoslavia and Iran. The END USER hereby gives its assurance to DVSI that it will not knowingly, unless prior authorization is obtained from the appropriate U.S. export authority, export or re-export, directly or indirectly to any of the restricted countries any products or technical data received from DVSI under this Agreement in violation of said United States Export Laws and Regulations. DVSI neither represents that a license is not required nor that, if required, it will be issued by the U.S. Department of Commerce. Licensee shall assume complete and sole responsibility for obtaining any licenses required for export purposes.

12.0 Governing Law

12.1 This Agreement is made under and shall be governed by and construed in accordance with the laws of the Commonwealth of Massachusetts, except that body of law governing conflicts of law. If any provision of this Agreement shall be held unenforceable by a court of competent jurisdiction, that provision shall be enforced to the maximum extent permissible, and the remaining provisions of this Agreement shall remain in full force and effect.

1. Product Introduction

1.1 General Information

Digital Voice Systems Inc.'s AMBE-2020™ Vocoder Chip is an extremely flexible, high-performance, single chip, speech compression coder. It provides superior voice quality at low data rates. It provides a real-time, half-duplex implementation of the standard-setting AMBE® voice compression software algorithm. DVSI's patented AMBE® voice compression technology has been proven to outperform CELP, RELP, VSELP, MELP, ECELP, MP-MLQ, LPC-10, and other competitive technologies. Numerous evaluations have shown its ability to provide performance equal to today's digital cellular systems at under half the data rate. The AMBE® voice compression algorithm is used in applications throughout the world, including the next generation of digital mobile communication systems.

The AMBE-2020™ Vocoder chip provides a high degree of flexibility in selecting the speech and FEC (Forward Error Correction) data rates. The user can separately select these parameters in 50 bps increments for total rates from 2.0 kbps to 9.6 kbps. Typically for higher error rate channels, the user will apportion a greater percentage of the total bit rate to FEC coding. The AMBE-2020™ voice coder maintains natural voice quality and speech intelligibility at rates as low as 2.0 kbits/sec. The AMBE® algorithm's low complexity allows it to be fully integrated into a low cost, low power integrated circuit, the AMBE-2020™ Vocoder Chip.

The AMBE-2020™ Vocoder Chip offers similar features to DVSI's AMBE-1000™ Vocoder Chip allowing it to be incorporated into systems already designed for the AMBE-1000™ and is interoperable with other DVSI products. The AMBE-2020™ Vocoder Chip delivers improved performance and enhanced modes such as 4.0 kbps toll quality speech and convolutional FEC coding. Along with these enhancements the AMBE-2020™ Vocoder Chip employs a control interface along with the variable data rates and FEC selections.

1.2 Advantages

- Superior Voice Quality
- Low Cost
- No External Memory Required
- Robust to Bit Errors & Background Noise
- Variable Data Rates - 2.0 kbps to 9.6 kbps
- Variable FEC Rates - 50 bps to 7.2 kbps
- Very Low Power (65mW @ 3.3V, 0.11mW Deep Sleep)
- Compact Single Chip Solution: 100 pin TQFP

Features

- High Quality Low Data Rate Speech Coding
- DVSI's Half Duplex AMBE® Voice Coder
- Supports Data Rates of 2.0 kbps to 9.6 kbps in 50 bps increments
- User Selectable Forward Error Correction rates
- Viterbi Decoder (rate 1/4 or more)
- 16 Level Soft Decision Decoding
- Voice Activity Detection (VAD) / Comfort Noise Insertion
- Single and Dual Tone (DTMF) Detection and Generation
- Power-Down Mode
- Minimal algorithmic processing delay
- DTMF detection and regeneration with North American call progress tones

1.3 Typical Applications

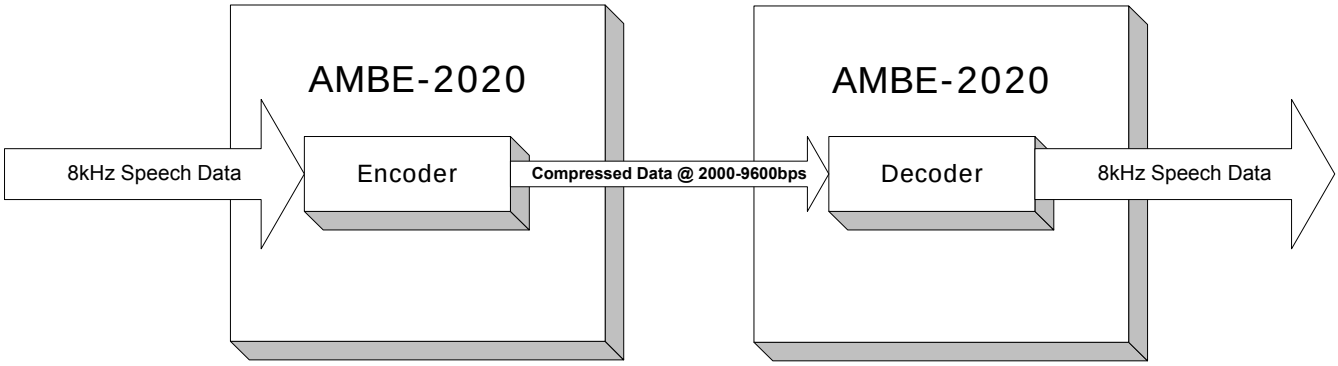
- Satellite Communications
- Digital Mobile Radio
- Secure Communications
- Cellular Telephony and PCS
- Voice Multiplexing
- Voice Mail
- Multimedia Applications

2 AMBE-2020™ Application Design Overview

2.1 Basic Operation

In its simplest model, the AMBE-2020™ can be viewed as two separate components, the **Encoder** and the **Decoder**. The Encoder receives an 8kHz sampled stream of *speech* data (16-bit linear, 8-bit Alaw, or 8-bit ulaw) and outputs a stream of *channel* data at the desired rate. Conversely the Decoder receives a stream of *channel* data and synthesizes a stream of *speech* data. The timing for the interfaces for the AMBE-2020™ Encoder and Decoder are fully asynchronous.

Figure 2-A Basic Operation



Typically the speech interface is an external A/D-D/A chip. The format of the incoming and outgoing speech data streams are coupled, that is to say they must be the same format (16-bit linear, 8-bit Alaw, or 8-bit μlaw). The channel interface is commonly (but not limited to) an 8 or 16 bit microprocessor or other suitable 'glue logic' hardware capable of performing the rudimentary formatting functions between the AMBE-2020™ channel format and the format of the system channel.

Optional functions of the chip, such as voice activation/detection, power mode control, data/FEC rate selection, etc. are controlled either through hardware control pins (see Section 5) and/or through the decoder command interface (see Section 4) Data sent into the decoder for function control purposes is distinguished from the data to be decoded into speech through a channel format which is described in Section 4.

2.2 Initial Design Considerations

Some of the initial design considerations the application engineer will face are the following:

- Choice of A/D-D/A chip.
- Choice of Channel Interface.
- Speech and FEC Rates.

2.2.1 A/D – D/A Overview

The choice of the A/D-D/A chip is critical to designing a system with superior voice quality. Given that Alaw and μlaw companding chips are already incorporating some compression to reduce the number of bits per sample, it is recommended that, when possible, a 16-bit linear device be used for maximum voice quality. When choosing a device, pay particular attention to Signal to Noise ratios and Frequency Responses of any filters that may be present on the analog front end of these chips. The Alaw and μlaw interfaces are also provided for the design engineer who is trying to fit to pre-existing conditions or is under other cost type restraints.

2.2.2 Vocoder Front End Requirements

In order to ensure proper performance from the voice coder, it is necessary for the vocoder front end to meet a set of minimum performance requirements. For the purposes of this section the vocoder front end is considered to be the total combined response between microphone/speaker and the digital PCM interface to the vocoder software, as shown in Figure 2-B. This includes any analog electronics plus the A-to-D and D-to-A converters as well as any digital filtering performed prior to the voice encoder or after the voice decoder.

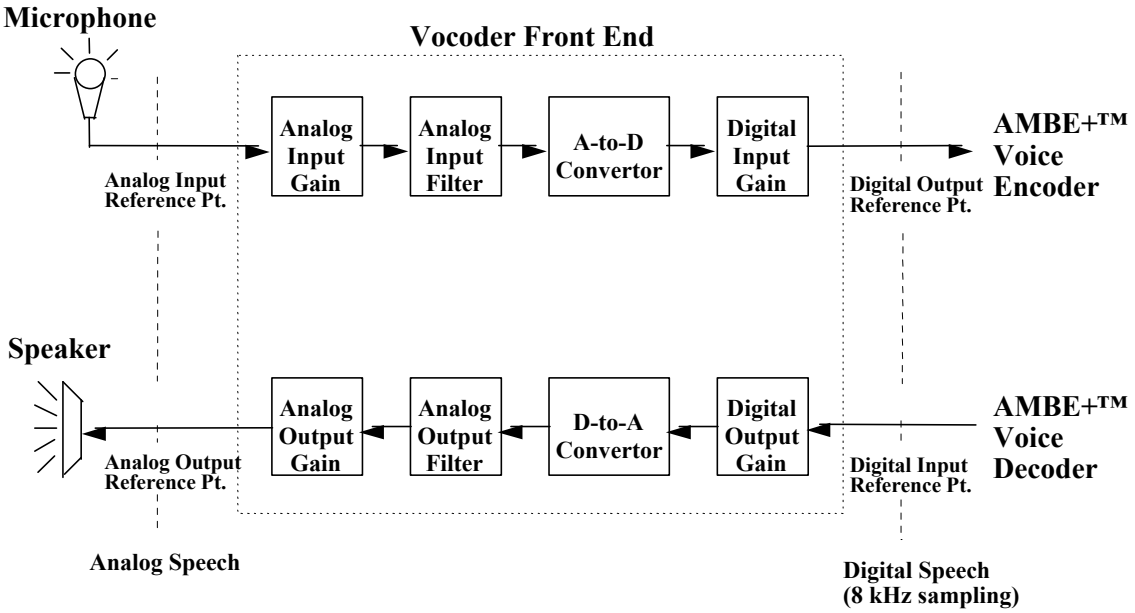


Figure 2 - B. Vocoder Front End

The AMBE+™ voice encoder and decoder operate with unity (i.e. 0 dB) gain. Consequently the analog input and output gain elements shown in Figure 2 are only used to match the sensitivity of the microphone and speaker with the A-to-D converters and D-to-A converters, respectively. It is recommended that the analog input gain be set such that the RMS speech level under nominal input conditions is 25 dB below the saturation point of the A-to-D converter (+3 dBm0). This level, which equates to -22 dBm0, is designed to provide sufficient margin to prevent the peaks of the speech waveform from being clipped by the A-to-D converter.

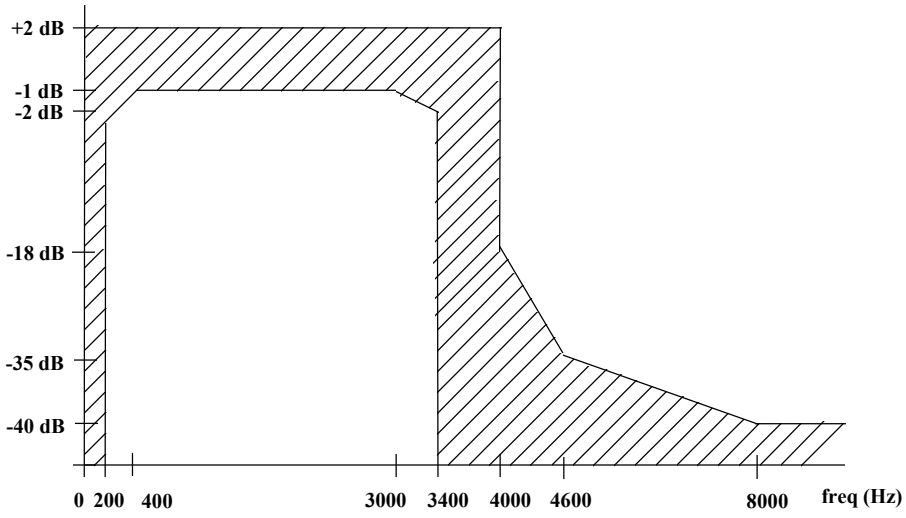


Figure 2 - C. Front End Input Filter Mask

The voice coder interface requires the A-to-D and D-to-A converters to operate at an 8 kHz sampling rate (i.e. a sampling period of 125 microseconds) at the digital input/output reference points. This requirement necessitates the use of analog filters at both the input and output to eliminate any frequency components above the Nyquist frequency (4 kHz). The recommended input filter mask is shown in Figure 2 - C, and the recommended output filter mask is shown in Figure 2 - D. For proper operation, the shaded zone of the respective figure should bound the frequency response of the front-end input and output.

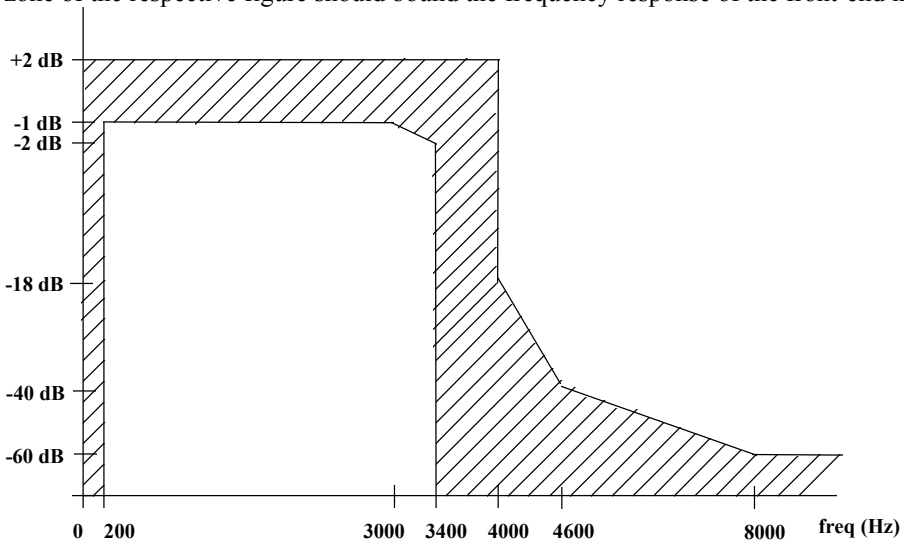


Figure 2 - D. Front End Output Filter Mask

This document assumes that the A-to-D converter produces digital samples where the maximum digital input level (+3 dBm0) is defined to be +/- 32767, and similarly, that the maximum digital output level of the D-to-A converter occurs at the same digital level of +/- 32767. If a converter is used which does not meet these assumptions then the digital gain elements shown in Figure 2 should be adjusted appropriately. Note that these assumptions are automatically satisfied if 16 bit linear A-to-D and D-to-A converters are used, in which case the digital gain elements should be set to unity gain. Also note that the vocoder requires that any companding which is applied by the A-to-D converter (i.e. alaw or ulaw) should be removed prior to speech encoding. Similarly any companding used by the D-to-A converter must be applied after speech decoding.

An additional recommendation addresses the maximum noise level measured at the output reference points shown in Figure 2-B with the corresponding inputs set to zero. DVSI recommends that the noise level for both directions should not exceed -60 dBm0 with no corresponding input. In addition the isolation from cross talk (or echo) from the output to the input should exceed 45 dB which can be achieved via either passive (electrical and/or acoustic design) or active (echo cancellation and/or suppression) means.

2.2.3 Channel Interface Overview

The channel interface is meant to be flexible to allow for easy integration with the system under design. The basic hardware unit of the interface is a serial port. The serial port can run in *passive* or *active* modes. In passive mode, all of the channel interface control signals are inputs to the AMBE2020™ chip. In active mode, only the TX_DATA_STRB is an output from the AMBE2020™ chip. All other signals are inputs.

Under normal operation, every 20ms, the encoder outputs a frame of coded bits, and the decoder needs to be delivered a frame of coded bits. There is some formatting of the data for both the encoder and the decoder. The primary purpose of the formatting is to provide alignment information for the encoded bit stream. The data has two formats, ***Framed*** and ***Unframed***. Serial mode can run in either **Framed** *or* **Unframed** mode.

The **Framed** and **Unframed** modes are explained in full detail in Section 4, but essentially the two formats are trying to achieve the same function, to provide positional information regarding the outgoing and incoming coded data streams. In **Framed** mode each 20msecs of output data from the encoder is preceded by a known structure (each packet corresponds to 20ms of speech data input into the encoder). This structure also embeds some status type flags, meant for local control

purposes, within it. The only data from the **Framed** format that is typically sent across the transmission channel under design are the actual encoded bits at the desired rate.

In **Framed** mode, it is the responsibility of the designed system to pass enough information along with the encoded bits such that the **Framed** format needed by the decoder can be reconstructed on the other side. This extra information, or overhead, is going to be very specific to the system under design, but at a minimum needs to pass enough information to reliably reconstruct the 20msec frame structure at the other end for the decoder.

In **Unframed** mode the data coming out of the encoder can be thought of as a continuous stream of voice data with the framing information embedded within the encoded bits. One advantage of this type of set-up is that the system does not have to add any bandwidth for overhead to the channel. The disadvantage is that the decoder needs 10-12 incoming frames in order to gain synchronization with the data stream before it can properly synthesize the speech waveform. Also, the **Unframed** mode only commits a single bit per frame to maintain data alignment. In higher error rate channels the performance will be improved by adding more bits per frame to the alignment information (which is more easily performed when using **Framed** mode).

Additional flexibility is given to the channel interface to the encoder and decoder by allowing the AMBE-2020™ Vocoder Chip to run in ***Passive*** or ***Active*** modes. In Passive mode, data strobes are provided by an external source, while in Active mode, data strobes are provided by the AMBE-2020™ Vocoder Chip. Serial interfaces can be run in Passive or Active modes. See Section 4 for full details and timing for both **Framed** and **Unframed** data.

2.2.4 Speech and FEC Rate Selection Overview

The total coded bit rate is the sum of two components, the Speech Data bit rate and the Forward Error Correction (FEC) Data bit rate. The addition of FEC data to the speech data allows the decoder to be able to correct a limited amount of errors within each frame should they arrive corrupted. If the channel is expected to have more errors then more bits should be dedicated to FEC. At the same time, voice quality will increase if the number of speech bits is increased.

3 Hardware Information

3.1 Special Handling Instructions

The AMBE-2020™ uses the TM320LC541B-66 core. For greater details on handling, electrical, packaging, or timing specs please refer to the TMS320-C54x data sheet at http://www.ti.com/sc/pcsheets/sprs039c/sprs039c.pdf.
Although the AMBE-2020™ Vocoder Chip incorporates input protection circuitry, to avoid damage from the accumulation of a static charge, industry standard electrostatic discharge precautions and procedures must be employed during handling and mounting.

The 100 pin TQFP package design of the AMBE-2020™ Vocoder Chip allows it to be mounted by infrared reflow, vapor-phase reflow or equivalent processes. The peak package body temperature must not exceed 220°C.
The AMBE-2020™ Vocoder Chip requires baking before mounting, if any of the following conditions exist:

- Humidity indicator card (included in packaging) shows exposure to > 20 % when read at 23°C + 5°C
- Devices were not shipped in a package designated as "moisture controlled."
- Not mounted within 168 hours of receipt, at factory conditions of ≤30°C and <60% RH
- If the device has not been stored at ≤ 20% RH

DVSI's recommended bake out procedures:

- For low-temperature device containers: 192 hours at 40°C + 5°C / -0°C and < 5% Relative Humidity
- For high-temperature device containers : 24 hours at 125°C + 5°C.

3.1.1 Storage

To insure maximum shelf life in long term storage, AMBE-2020™ Vocoder Chips should be kept in a moisture controlled package at <40°C and <90% Relative Humidity

3.2 Pin Descriptions

Pin Number	Pin Descriptive Name	Pin Direction	Notes
77	CHAN_SEL1	Input	Channel Interface Selection Pins: Use these bits to select the channel interface type (framed, unframed active, passive) according to Table 4-A. See full description in section 4.2.
75	CHAN_SEL0	Input	Used with CHAN_SEL1 to select channel operation mode
85	CODEC_SEL1	Input	A/D-D/A Select Pins see Table 6-A to select the interface.
84	CODEC_SEL0	Input	
74	RATE_SEL4	Input	Coding Rate Select Pins: Use these bits to select the voice and FEC rates according to section 7.2. The coding rates are also selectable using the Control Word interface described in section 5.2.4.
73	RATE_SEL3	Input	
72	RATE_SEL2	Input	
71	RATE_SEL1	Input	
70	RATE_SEL0	Input	
86	VAD_EN	Input	Voice Activation Detection Enable Pin. Active HIGH. See Section 7.3. VAD can also be enabled/disabled using the Control Word interface as described in section 5.2.9.
24	ENCODER_EN	Input	Encoder/Decoder switch. Switch on to enable Encoder and disable Decoder (must be used in conjunction with Encoder Enable function in Framed Input. See Section 5.2.9). Switch off to enable Decoder and disable Encoder.
83	SLEEP_EN	Input	Standard Sleep Enable Pin. Active HIGH. See Section 7.5.1.
82	SLIP_EN	Input	Slip Control Enable Pin. Active HIGH. See Section 7.6.
68	X2/CLKIN	Input	Clock Input 1. 16.384 MHz input. See Section 3.3
67	X1	Input	Output from internal oscillator for the crystal. If the internal oscillator is not used this pin should be unconnected.
69	RESETN	Input	AMBE-2020™ Reset pin. Active LOW. See Section 3.3
20	EPR	Output	Encode Packet Ready: Following a reset, this signal will have a high to low transition to indicate the first packet is ready. The next packet will be ready approximately 20 msec later. **See Note 1.**
79	SOFT_EN	Input	Soft decision decoding enable. When high it enables 4 bit soft decision error decoder. Keep low when not in use.
80	BAUD_SEL0	Input	Baud Rate Selector for unframed serial mode See Table 4-B.
81	BAUD_SEL1	Input	
32	CHAN_RX_DATA	Input	Channel Receive Data to AMBE-2020™
42	CHAN_TX_DATA	Output	Channel Transmit Data from AMBE-2020™
28	CHAN_RX_CLK	Input	Channel Receive Clock
34	CHAN_TX_CLK	Input	Channel Transmit Clock
38	CHAN_TX_STRB	I/O	Channel Transmit Data Strobe
30	CHAN_RX_STRB	Input	Channel Receive Data Strobe
29	CODEC_RX_STRB	Input	Frame synchronization pulse for A/D data. Should be connected to CODEC_TX_STRB
37	CODEC_TX_STRB	Input	Frame synchronization pulse for D/A data. Should be connected to CODEC_RX_STRB
31	CODEC_RX_DATA	Input	PCM Data from A/D Converter to AMBE-2020™

Pin Number	Pin Descriptive Name	Pin Direction	Notes
41	CODEC_TX_DATA	Output	PCM Data from AMBE-2020™ to D/A Converter
27	CODEC_RX_CLK	Input	A/D Serial clock. Should be connected to CODEC_TX_CLK
33	CODEC_TX_CLK	Input	D/A Serial clock Should be connected to CODEC_RX_CLK
51	CLOCK_MODE	Input	If high enables crystal oscillator option for clock source. If low then external oscillator option is selected. See Section 3.5 for details.
8,11,12,23, 36,39,44,45, 46,47,48, 49,54,57, 64,76,87,90	VDD	Power	Supply Voltage
1,9,10,25, 26,35,40,50, 52,53,56, 63,65,88,89	GND	Power	Ground
2,3,4,5,6,7, 13,14,15,16, 17,18,19,21, 22,43,55,58, 59,60,61,62, 66,78,91,92, 93,94,95,96, 97,98,99, 100	No Connection		These pins must remain unconnected

NOTE 1: The AMBE-2020™ expects an encoder packet to be read approximately every 20 msec. Following the initial reset, wait for EPR to go low and read the initial packet (t_0). 20 msec later, the next packet (t_1) should be ready. For packet t_1 and all following packets use the procedure below:

1) Wait for slightly less than 20 msec.
2) Assert CHAN_TX_STB and read word on CHAN_TX_DATA.
3) If transmitted word not 0x13EC, discard it and repeat step 2.
4) If transmitted word 0x13EC, read 23 more words (rest of packet).

The EPR signal should not be used as an interrupt. The EPR is only valid for the first high to low transition.
A new packet should be ready every 20 msec after the initial EPR high to low transition. A packet read should take place every 20 msec. If there is a delay in the read (i.e. a packet is missed), it is recommended that the device be reset.

NOTE 2: To prevent possible damage to the chip be sure that your circuit meets the following three requirements.

1) No signals should be applied to the device (this includes clocks) before the power is applied.
2) The clock and reset must be applied to the device during power up. If the clock and reset are not applied during power up, high currents may flow damaging the device.
3) All of the configuration I/O pins of the device should be pulled up or pulled down through individual 10 K ohm resistors to limit current flow through the I/O sections. See Table below for the affected pins.

Descriptive Name	Pin Number		Descriptive Name	Pin Number
CHAN_SEL1	77		VAD_EN	86
CHAN_SEL0	75		ENCODER_EN	24
CODEC_SEL1	85		SLEEP_EN	83
CODEC_SEL0	84		SLIP_EN	82
RATE_SEL4	74		SPFT_EN	79
RATE_SEL3	73		BAUD_SEL0	80
RATE_SEL2	72		BAUD_SEL1	81
RATE_SEL1	71			
RATE_SEL0	70			

3.3 Clock and Reset Timing

To reset the AMBE-2020™ chip, the reset signal must be held low for a minimum of 50 µs. The recovery time from reset is approximately 95 msec. In other words, 95 msec after the rising edge of the reset signal the AMBE-2020™ starts processing PCM samples. The first packet will be ready after 252 PCM samples are read.

Figure 3-A X2/CLKIN and CLKOUT Timing Diagram

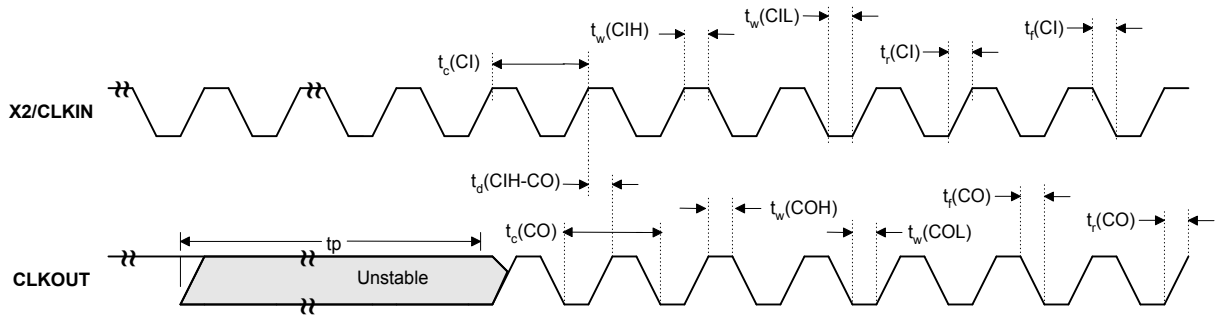


Table 3-A X2/CLKIN and CLKOUT Timing Parameters

Reference	Parameter		Min	Max	Units
t_c(CI)	Cycle time, X2/CLKIN	Integer PLL multiplier N (N=4)	20	400	ns
t_f(CL)	Fall time, X2/CLKIN			4	ns
t_r(CL)	Rise time, X2/CLKIN			4	ns
t_w(CIL)	Pulse duration, X2/CLKIN low		6		ns
t_w(CIH)	Pulse duration, X2/CLKIN high		6		ns
t_P	Transitory phase, PLL lock-up time			50	µs
t_c(CO)	Cycle time, CLKOUT (typical is t_c(CI)/4)		15		ns
t_d(CIH-CO)	Delay time, X2/CLKIN high/low to CLKOUT high/low		4	16	ns
t_f(CO)/t_r(CO)	Fall/Rise time, CLKOUT (typical is 2 ns)				
t_w(COL)	Pulse duration, CLKOUT low		H-4	H	ns
t_w(COH)	Pulse duration, CLKOUT high		H-4	H	ns

- CLKOUT is shown for reference only it is not connected.
- H=7.629 ns

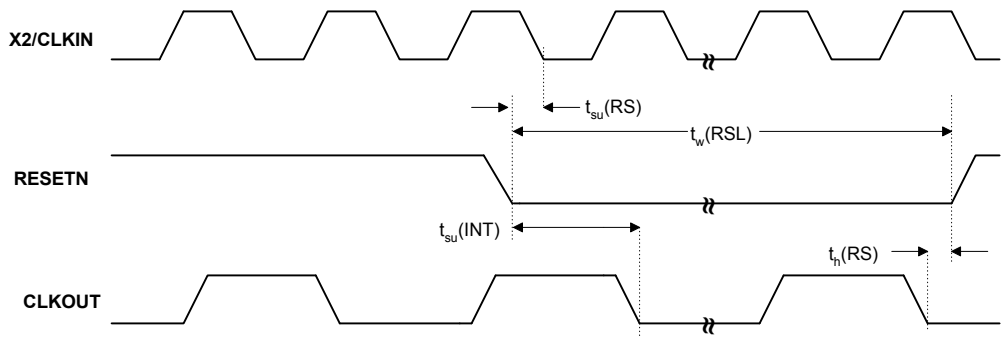


Figure 3-B Hardware Reset Timing Diagram

Figure 3-C Hardware Reset Timing DiagramTable 3-B Reset Timing Parameters

Reference	Parameter	Min	Max	Units
t_h(RS)	Hold time, RS after CLKOUT low	0		ns
t_w(RSL)	Pulse duration, RS low	50		µs
t_{su}(RS)	Setup time, RS before X2/CLKIN low	5		ns
t_{su}(INT)	Setup time, INTn, NMI, RS before CLKOUT low	10		ns

- CLKOUT is shown for reference only it is not connected.

3.4 Associated Chip Delay

The associated delay due to the coding/decoding algorithm is shown below

Encoder Delay

Algorithmic Delay = 32 ms
Encoder Processing Delay = 11.5 ms

Decoder Delay

Algorithmic Delay = 10 ms
Decoder Processing Delay = 7.5 ms

Total Delay = 32 ms + 11.5 ms + 1 ms* +10 ms +7.5 ms = 62 ms

Frame Processing Delay = 11.5 ms (encoder) + 1 ms* + 7.5 ms = 20 ms

- 1ms of idle time between encode and decode sequence.

3.5 Crystal / Oscillator Usage

The AMBE-2020™ Vocoder Chip has an input clock frequency of 16.384 MHz. Two options are outlined below in providing this signal. The CLOCK_MODE pin 51 must be set appropriately for the option used.

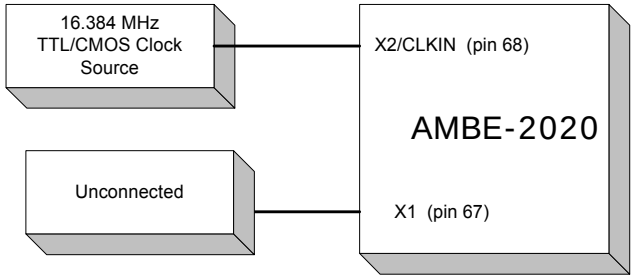
The following points should be noted when designing any printed circuit board layout:

- Keep the crystal and external capacitors as close to the X2/CLKIN and X1 pins as possible to minimize board stray capacitance.
- Keep X2/CLKIN and X1 away from high frequency digital traces (example CLKOUT) to avoid coupling.

3.5.1 TTL Clock Source

If CLOCK_MODE pin is low then a TTL/CMOS source is used as the clock input. Connect X2/CLKIN and X1 as follows:

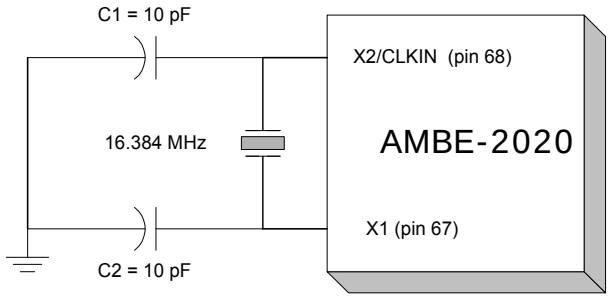
Figure 3-D X2/CLKIN and X1 with TTL Clock Source



3.5.2 Crystal Oscillator

The Crystal Oscillator option is selected with CLOCK_MODE pin set to a high level. To use the crystal oscillator, connect the crystal across X2/CLKIN and X1 along with one external capacitor from each of these pins to ground. Recommended values for C1 and C2 is 10 pF.

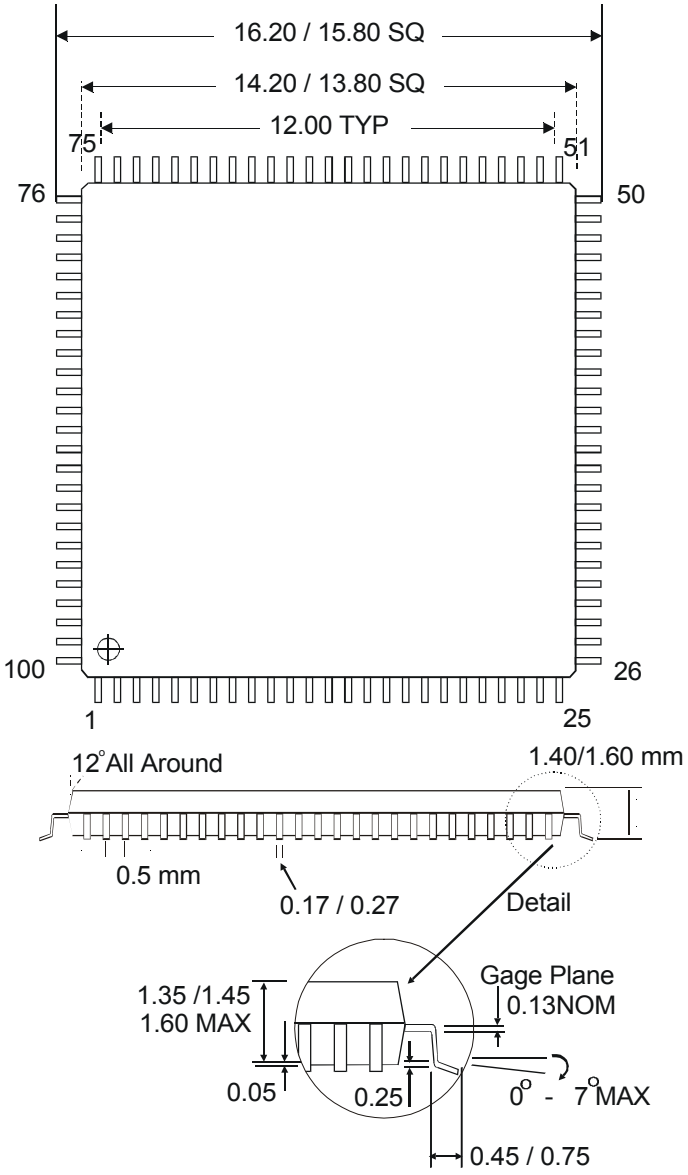
Figure 3-E X2/CLKIN and X1 with Crystal Oscillator



3.6 Package Description

100 pin TQFP (Thin Quad Flat Pack)
All Dimensions are in millimeters

Figure 3-F Package Dimensions



Not Drawn to Scale

Figure 3-G Package Dimensions

AMBE-2020-10 = The DVSI device part number.

DVSI = Digital Voice Systems, Incorporated

D16877PZ-66 = Internal Texas Instruments part number for the AMBE-2020

A = WF Code

D = Die Rev Code

W = Die Shrink Code

43AT3FW = Lot Trace Code

43 = 2 Digit YR/MO Code (Updated Monthly)
AT3F = Assy Lot
W = Assy Site Code

3.7 Normal Operating Conditions

Table 3-C Normal Operating Conditions

Normal Operating Conditions	
Operating Voltage	3.3V
Operating Case Temperature Range	-40°C to 100°C
Storage Temperature Range	-55°C to 150°C

3.8 Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can aversely affect device reliability.

Table 3-D Absolute Maximum Ratings

Absolute Maximum Ratings	
Voltage Range on any Pin with Respect to Ground	-0.3V to 4.6V

3.9 Electrical Characteristics and Requirements

Table 3-E Recommended Operating Conditions

Parameter			Min	Nom	Max	Unit
DV_{DD}	Device Supply Voltage		3	3.3	3.6	V
V_{SS}	Supply Voltage, GND		-	0	-	V
V_{IH}	High-level input voltage, I/O	RESETN (pin 69), CLOCK_MODE (pin 51), X2/CLKIN (pin 68), pins 44,45,46,47,48,52,53,54 DV_{DD} = 3.3 ±0.3 V	2.5	-	DV_{DD} + 0.3	V
		All other inputs	2.0			
V_{IL}	Low-level input voltage		-0.3	-	0.8	V
I_{OH}	High-level output current		-	-	-300	µA
I_{OL}	Low-level output current		-	-	1.5	mA

Table 3-F Electrical Characteristics over Recommended Operating Case Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions	MIN	TYP†	MAX	Unit
V_{OH} High-level output voltage‡	V_{DD} = 3.3 ±V, I_{OH} = MAX	2.4			V
V_{OL} Low-level output voltage‡	I_{OL} = MAX			0.4	V
I_X Input current in high impedance (V_I = V_{SS} to V_{DD})	V_{DD} = MAX, V_I = V_{SS} to V_{DD}	-10		10	µA
C_I Input capacitance			10		pF
C_O Output capacitance			10		pF

† All values are typical unless otherwise specified.

3.10 Thermal Resistance Characteristics

Thermal Resistance Characteristics	
R_{TJA}	58 °C/W
R_{TJC}	10 °C/W

Table 3G Thermal Resistance Characteristics

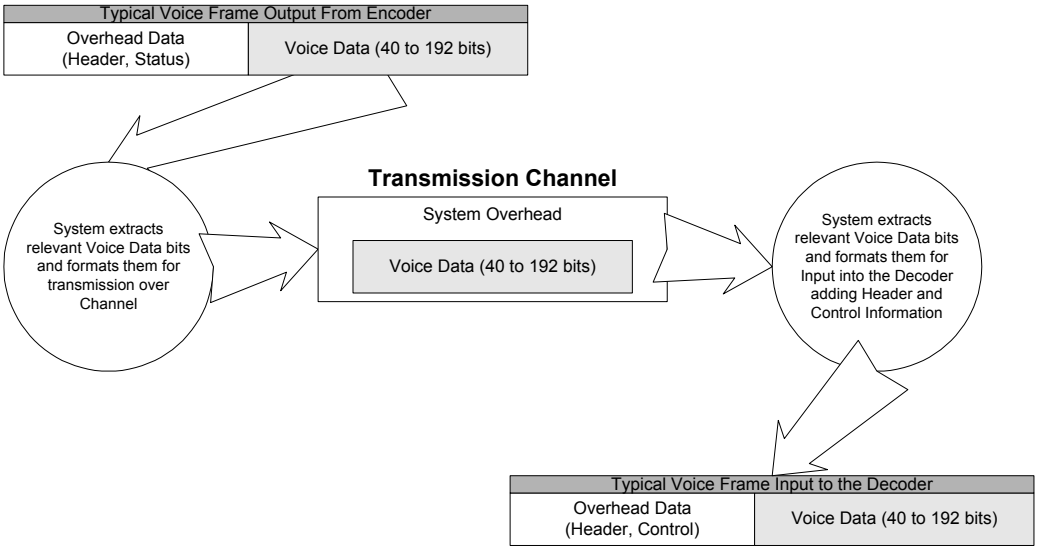
4 Channel Interface

4.1 Overview

The Channel Interface is the general term used for the interface for the compressed bits coming from the encoder and the compressed bits going to the decoder. This same interface is also used to output *status* information from the encoder and decoder such as whether a DTMF tone has just been detected in the speech input, or whether the decoder has detected and synthesized a frame of silence. Additionally, this interface is used to perform more complex control operations on both the encoder and decoder (usually at start-up). These control functions include speech data and FEC rate control.

It is important to realize that not all data being output from the AMBE-2020™ is intended for transmission over the channel. Status type of data is typically only useful at the 'local' end. In most voice transmission systems, the actual encoded bits are extracted from the channel formatting, combined into the systems transmission stream, sent over the transmission path, extracted from the transmission path at the receiving end, and reassembled into the AMBE-2020™ 's channel format for synthesis by the decoder.

Figure 4-A Channel Interface Overview



4.2 Serial Configuration Selection

The hardware interface to the Channel Interface is configured as a serial interface based exclusively on the hardware settings of CHAN_SEL[1-0]. See Table 4-A.

Table 4-A Channel Interface Selection Table

Port Type	Interface Select Pins	
	CHAN_SEL1 (pin 77)	CHAN_SEL0 (pin 75)
Active Framed	0	0
Active Unframed	0	1
Passive Framed	1	0
Passive Unframed	1	1

Table 4-B Unframed Bit per Word Selection Table

Number of Voice Data Bits per Word	Interface Select Pins	
	BAUD_SEL1 (pin 81)	BAUD_SEL0 (pin 80)
1	0	0
2	0	1
3	1	0
4	1	1

All transfers occur through a serial port. The serial port inputs and outputs a 16 bit word for every write and read strobe signal respectively. Serial mode can be **framed** or **unframed**. Within the **unframed** mode, the data is input and output in 16 bits words still but with only 1 to 4 voice data bits carried within each word. These four configurations can be seen in Table 4-B. See section 4.3 for all the details on the serial interface.

4.3 Channel Serial Mode

The signals in Table 4-C make up the serial channel interface. The serial channel mode transfers data in and out of the AMBE-2020™ using 16 bit words on the two data lines **CHAN_RX_DATA** and **CHAN_TX_DATA**. The selection of the **framed** or **unframed** format of this data is made using information in Table 4-A.

Table 4-C Channel Serial Interface Pin Descriptions

Pin Symbol	Pin Direction	Pin Number	Description
EPR	Out	20	**Encoder Packet Ready**: Following a reset, this output signal will have a high to low transition to indicate that the encoder has a frame of data to output. The next packet will be ready approximately 20 msec later. **See Note 1.**
CHAN_RX_DATA	In	32	**Serial Data Input** : 16 bits of channel data are input on **CHAN_RX_DATA**, synchronous to **CHAN_RX_CLK**, with each **CHAN_RX_STRB** pulse.
CHAN_RX_CLK	In	28	**Serial Input Clock** : In coordination with **CHAN_RX_STRB**, **CHAN_RX_DATA** is latched by the AMBE-2020™ on the falling edges of **CHAN_RX_CLK**.
CHAN_RX_STRB	In	30	**Input (Write) Data Strobe** : This signal indicates to the AMBE-2020™ when the data on **CHAN_RX_DATA** will be latched by **CHAN_RX_CLK**. See figure 4-B.
CHAN_TX_DATA	Out	42	**Serial Data Output** : 16 bits of channel data are output on **CHAN_TX_DATA**, synchronous to **CHAN_TX_CLK**, with each **CHAN_TX_STRB** pulse.
CHAN_TX_CLK	In	34	**Serial Output Clock** : In coordination with **CHAN_TX_STRB**, the data on **CHAN_TX_DATA** is output by the AMBE-2020™ on the rising edges of **CHAN_TX_CLK**.
CHAN_TX_STRB	Active Output/ Passive Input	38	**Output (Read) Data Strobe** : This signal indicates to the AMBE-2020™ when to bring the data to the **CHAN_TX_DATA** pin. See figure 4-B.

Note 1: The AMBE-2020™ expects an encoder packet to be read approximately every 20 msec. Following the initial reset, wait for EPR to go low and read the initial packet (t0). 20 msec later, the next packet (t1) should be ready. For packet t1 and all following packets use the procedure below:

1) Wait for slightly less than 20 msec.
2) Assert CHAN_TX_STB and read word on CHAN_TX_DATA.
3) If transmitted word not 0x13EC, discard it and repeat step 2.
4) If transmitted word 0x13EC, read 23 more words (rest of packet).

A new packet should be ready every 20 msec after the initial EPR high to low transition. A packet read should take place every 20 msec. If there is a delay in the read (i.e. a packet is missed), it is recommended that the device be reset.

4.3.1 Low Level Timing for Passive and Active Serial Mode

Figure 4-B Low Level Timing for Passive and Active Serial Mode

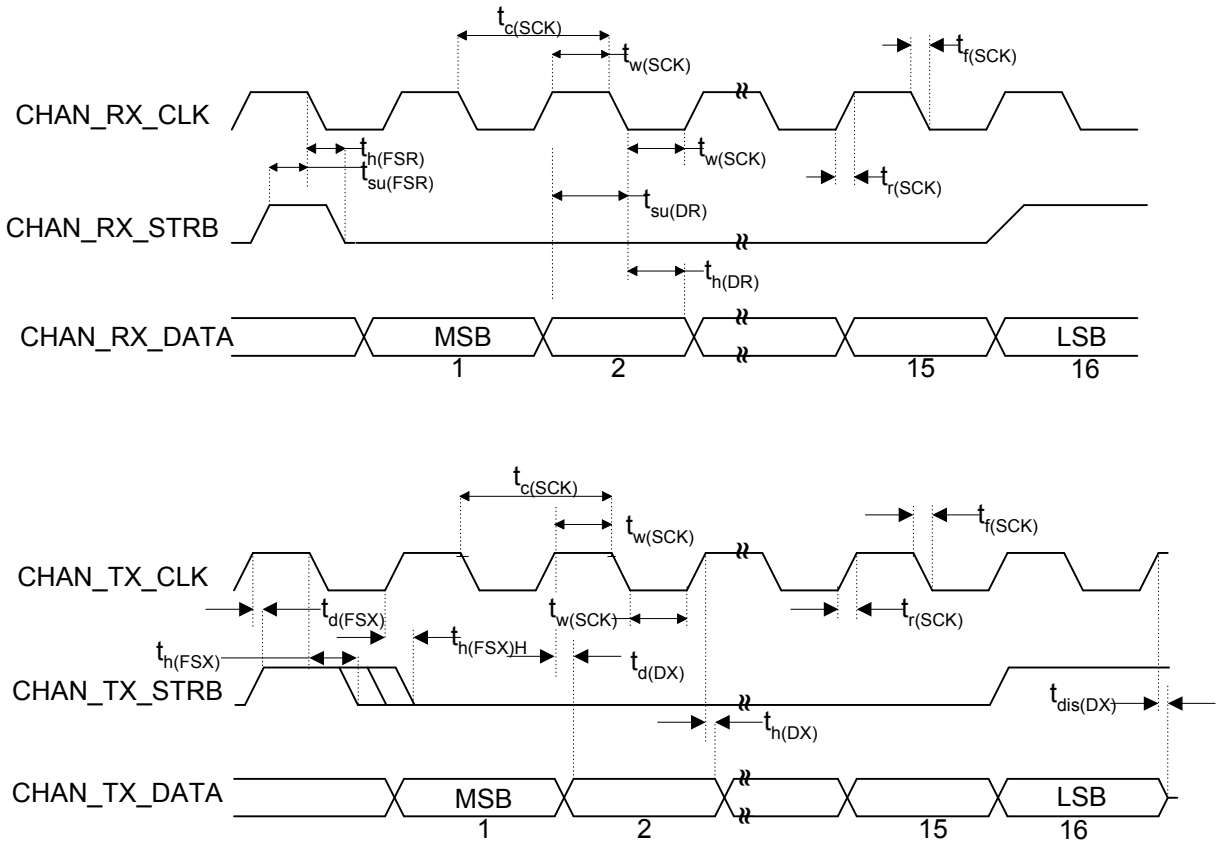


Table 4-D Switching Characteristics Over Recommended Operating Conditions for Serial Port Receive

Reference	Parameter	3.3 Volts		Units
		Min	Max	
$t_{h(FSR)}$	Hold time, FSR after CLKR falling edge	6		ns
$t_{h(DR)}$	Hold time, DR after CLKR falling edge	6		ns

Table 4-E Switching Characteristics Over Recommended Operating Conditions for Serial Port Receive

Reference	Parameter	3.3 Volts		Units
		Min	Max	
$t_{d(DX)}$	Delay time, DX valid after CLKX rising (Passive Mode)		25	ns
$t_{c(SCK)}$	Cycle time, serial port clock	6H		ns
$t_{f(SCK)}$	Fall time, serial port clock		6	ns
$t_{r(SCK)}$	Rise time, serial port clock		6	ns
$t_{w(SCK)}$	Pulse duration, serial port clock low/ high	3H		ns
$t_{su(FSR)}$	Setup time, FSR before CLKR falling edge	6		ns
$t_{su(DR)}$	Setup time, DR before CLKR falling edge	6		ns
$t_{d(FSX)}$	Delay time, CLKX rising to FSX		15	ns
$t_{d(DX)}$	Delay time, CLKX rising to DX (Active Mode)		15	ns
$t_{h(FSX)}$	Hold time, FSX after CLKX falling edge	6		ns
$t_{h(FSX)H}$	Hold time, FSX after CLKX rising edge		2H-5	ns
$t_{dis(DX)}$	Disable time, CLKX rising to DX		20	ns
$t_{h(DX)}$	Hold time, DX valid after CLKX rising edge	-5		ns

- Note: H = 7.629 ns; however, do not operate serial clocks any faster than 2.048 MHz. Thus $t_{c(SCK)}$ should be a minimum of 488.3 nsec.

5 Channel Data Format

The channel interface is responsible for outputting the compressed data from the encoder and inputting compressed data to the decoder. In addition to these most basic functions the channel interface is also capable of reporting certain events, such as the detection of a DTMF tone. The channel interface can also control certain selectable functions of the AMBE-2020™, such as the voice coding rate. This chapter will describe how the AMBE-2020™ uses the channel interface to multiplex these capabilities.

There are two formats to the data, **Framed** and **Unframed**, both of which operate in serial mode. Generally speaking the **Unframed** mode is used only when the connection between the AMBE-2020™ and the channel under design is relatively direct, and the designer wants to simplify the extraction of the relevant voice data. In this mode configuration is accomplished using hardwired pins. In most cases, when a controller is present between the AMBE-2020™ and the channel, the system designer will find that using the **Framed** format is more flexible.

5.1 Framed Format

The **Framed** format is a 24 by sixteen-bit word format for a total of 48 bytes or 384 bits. Every 20 milliseconds either the encoder outputs 24 sixteen-bit words, or the decoder expects to receive 24 words depending which mode the chip is in (encode only or decode only). The format of the input and output frames are detailed below. The first 12 sixteen bit words are made up of header, ID and status or control information. The remaining 12 sixteen bit words make up the encoded data bit field. These 12 words, or 192 bits, will be fully populated with relevant voice data only when the AMBE-2020™ is operating in a 9600bps mode (9600 bits/sec ÷ 50 frames/sec = 192 bits/frame). Otherwise, when the data rate is less than 9600bps, the coded voice bits are filled starting from the MSB of the first word in the field, leaving any unused bits as zeros. It is important to note here that even when the AMBE-2020™is operating at less than 9600bps, *all* 384 bits of the **Framed** format (including any unused trailing zeros) must be transferred out of the encoder and into the decoder.

5.2 Framed Input Format

In Figure 5-A we see the format of the **Framed** input. Keep in mind that even though the channel data in this **Framed** input format is closely associated with the decoder, the control information will apply to both encoder *and* decoder functions.

Figure 5-A Basic Framed Input Format

20 ms frame	24 sixteen-bit words = 48 bytes = 384 bits		Word #	Description	
		(12) 16 bit words of overhead (192 bits)	0	Header always set to 0x13EC	
			1	Power Control ID (8bits)	Control Word 1 (8 bits) – see Table 5-B
			2	Rate info 0	See Tables 5-C and 5-D
			3	Rate info 1	
			4	Rate info 2	
			5	Rate info 3	
			6	Rate info 4	
			7	Unused in Input	
			8	Unused in Input	
			9	Unused in Input	
			10	DTMF Control – see Tables 5-E and 5-F	
			11	Control Word 2 – see Table 5-G	
		(12) 16 bit words of data (192 bits)	12	Channel Data	
			13	Channel Data	
			14	Channel Data	
			15	Channel Data	
			16	Channel Data	
			17	Channel Data	
			18	Channel Data	
			19	Channel Data	
			20	Channel Data	
			21	Channel Data	
			22	Channel Data	
			23	Channel Data	

5.2.1 Framed Input: Word 0 : Header

The decoder uses the header information to synchronize with the beginning of each 20 millisecond frame. this 16 bit word **MUST** be **0x13EC**.

5.2.2 Framed Input: Word 1 : Power Control ID

Set the 8-bit Power Control ID field to 0x00 for normal use. For Power Down Mode, set this value to **0x55**. This causes the AMBE-2020™ to enter low power mode. To exit low power mode, the device must be reset through the hardware.

Table 5-A Framed Input : Power Control ID Values Summary

ID	Type	Description
0x00	Voice Data	This ID value instructs AMBE-2020™ to operate in normal fashion
0x55	Low Power Mode	When this mode is activated the AMBE-2020™ Vocoder Chip will go into a mode which conserves power, where no voice packets are being processed.

5.2.3 Framed Input: Word 1 : Control Word 1

Use the 8-bit control word to set various functions.

Table 5-B Control Word 1 Format

Control Word 1 – 8-bits (See Table 1-F)							
7: MSB	6	5	4	3	2	1	0 : LSB
Lost Frame Indicator	Unused	Unused	Unused	Unused	Unused	**CNI**	Unused

Lost Frame Indicator : Setting the Lost Frame Indicator bit to a 1 will cause the AMBE-2020™ decoder to construct the voice frame using the parameters from the previous frame. This is an effective way to mask the effects of short periods of data loss. This bit should be set by the user when channel data is lost or corrupted. It works by replacing the frame of corrupted data with the previous, intact, frame.

Comfort Noise Insertion (CNI) : Setting the CNI bit will cause the decoder to output a frame of comfort noise. This bit is used with systems that are capable of discontinuous transmission (DTX).

5.2.4 Framed Input: Words 2-6 : Rate Information

Rate Info 0, Rate Info 1, Rate Info 2, Rate Info 3, Rate Info 4

The initial rate of the AMBE-2020™ is set through the hardware pins RATE_SEL[4-0] (see Section 7.2 and Tables 7-A and 7-B) after resetting the device. The coding rate can be modified for both the encoder and the decoder by sending a framed packet to the input channel interface. The Rate Selector control field (described in section 5.2.9) determines where to apply the rate change. Particular attention must be paid to this field when using the BER reporting fields (section 5.3).

The AMBE-2020™ used these five words to set the source and FEC coding rates. Tables 5-C and 5-D list predefined value for various source and FEC rates. These are only a representation of the most common rates that are requested. Please contact DVSI for additional rate information if the desired rates are not listed. The software configurations in Table 5-C are compatible for use with the AMBE-1000™ (using AMBE™ technology). If compatibility is not an issue, use the software codes in Table 5-D to select speech and FEC rates to optimize use of the AMBE-2020™ (using AMBE+™ technology).

Table 5-C Rate Selection Using Rate Info 0-4, compatible w/ AMBE-1000™ (AMBE)

Rate Info 0	Rate Info 1	Rate Info 2	Rate Info 3	Rate Info 4	Speech Rate (bps)	FEC Rate (bps)	Total Rate (bps)
0x9030	0x0000	0x0000	0x0000	0x4330	2400	0	2400
0x902f	0x0000	0x0000	0x0000	0x6930	2350	50	
0x9348	0x0000	0x0000	0x0000	0x6f48	3600	0	3600
0x9243	0x0080	0x0000	0x0000	0x5348	3350	250	
0xab50	0x0000	0x0000	0x0000	0x3950	4000	0	4000
0x934b	0x0080	0x0000	0x0000	0x3950	3750	250	
0xab60	0x0000	0x0000	0x0000	0x7960	4800	0	4800
0xab5b	0x0080	0x0000	0x0000	0x6860	4550	250	
0x9348	0x2030	0x0000	0x0000	0x7060	3600	1200	
0x923e	0x2800	0x0000	0x0000	0x7460	3100	1700	
0xab53	0x2c00	0x0000	0x0000	0x5680	4150	2250	6400
0xab58	0x3000	0x0000	0x0000	0x4490	4400	2800	7200
0xbf9b	0x0080	0x0000	0x0000	0x49a0	7750	250	8000
0xab5d	0x3400	0x0000	0x0000	0x31a0	4650	3350	
0xbfc0	0x0000	0x0000	0x0000	0x72c0	9600	0	9600
0xab16	0xe400	0x0000	0x0000	0x67c0	4850	4750	

Table 5-D Rate Selection Using Rate Info 0-4, AMBE-2020™ only (AMBE+)

Rate Info 0	Rate Info 1	Rate Info 2	Rate Info 3	Rate Info 4	Speech Rate (bps)	FEC Rate (bps)	Total Rate (bps)
0x0028	0x0000	0x0000	0x0000	0x6428	2000	0	2000
0x5048	0x0000	0x0000	0x0000	0x3948	3600	0	3600
0x1030	0x0001	0x0000	0x4230	0x0048	2400	1200*	
0x1030	0x4000	0x0000	0x0000	0x0048	2400	1200**	
0x5250	0x0000	0x0000	0x0000	0x4150	4000	0	4000
0x1030	0x0001	0x0000	0x341a	0x6750	2400	1600	
0x5360	0x0000	0x0000	0x0000	0x6c60	4800	0	4800
0x5250	0x2010	0x0000	0x0000	0x7460	4000	800	
0x5048	0x0001	0x0000	0x2412	0x6860	3600	1200	
0x1030	0x0005	0x180c	0x3018	0x7360	2400	2400	
0x6b80	0x0000	0x0000	0x0000	0x6c80	6400	0	6400
0x5250	0x0001	0x0000	0x542a	0x5280	4000	2400	
0x5258	0x0009	0x1e0c	0x4127	0x7390	4400	2800	7200
0x7fa0	0x0000	0x0000	0x0000	0x52a0	8000	0	8000
0x5250	0x0005	0x2010	0x6834	0x72a0	4000	4000	
0x7fc0	0x0000	0x0000	0x0000	0x69c0	9600	0	9600
0x5048	0x000e	0x4010	0x6a2e	0x65c0	3600	6000	
0x1030	0x000e	0x681a	0x511b	0x76c0	2400	7200	

* FEC is a convolutional code
** FEC is a block code

5.2.5 Framed Input: Word 7 : Unused in Input

Should be set to 0x0000

5.2.6 Framed Input: Word 8 : Unused in Input

Should be set to 0x0000

5.2.7 Framed Input: Word 9 : Unused in Input

Should be set to 0x0000

5.2.8 Framed Input: Word 10 : DTMF Control

Use this word to set DTMF tones. See Table 5-F for a list of tones and their corresponding values.

Table 5-E DTMF Control Format

DTMF Control – 16-bits															
15: MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0: LSB
DTMF Amplitude								DTMF Digit Detect/ Generate							

Table 5-F DTMF Codes for Digit Detect/ Generate

DTMF Code	DTMF Digit	Frequency 1 (Hz)	Frequency 2 (Hz)
0x80	1	1209	697
0x84	2	1336	697
0x88	3	1477	697
0x81	4	1209	770
0x85	5	1336	770
0x89	6	1477	770
0x82	7	1209	852
0x86	8	1336	852
0x8A	9	1477	852
0x87	0	1336	941
0x83	*	1209	941
0x8B	#	1477	941
0x8C	A	1633	697
0x8D	B	1633	770
0x8E	C	1633	852
0x8F	D	1633	941
0xff	Inactive	N/A	N/A

To generate no tones, set the DTMF Code to 0xff. Dial, ring, and busy tones are standard North American call progress tones. An expanded list of tones and values can be found in the Appendices, Section 8.4.

DTMF Amplitude

The DTMF Amplitude runs from 3 to –60 dBm0. The value is a signed byte. So 0x03 = 3, 0x00 = 0, 0xff = -1, 0xc4 = -60.

5.2.9 Framed Input: Word 11 : Control Word 2

Table 5-G Control Word 2 Format

Control_Word 2 – 16-bits															
Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Decoder Output Volume Control								Unused 0	Unused 0	VAD	Unused 0	SL	EE	RIS	

Decoder output volume control

The default gain value is set to 0x80h

Rate Information Selector (RIS) :
Use these 2 bits to select which part(s) of the vocoder will be affected by the rate selection words.

Table 5-H Rate Information Selection Codes

value	Area Controlled
0x0	Encoder and Decoder
0x1	Encoder only
0x2	Decoder only
0x3	Neither Encoder nor Decoder

Encoder Enable (EE):
Set this bit to 1 AND set the Encoder Enable Pin (ENCODER_EN, pin 24, see section 3.2) to 1 to enable the encoder and disable the decoder on a frame by frame basis. Set this bit to 0 to enable the decoder and disable the encoder. This must be set to the desired function in every packet sent to continue use.

Sleep (SL):
Set this bit to 1 to enter Sleep mode on a frame by frame basis. Sleep is a low power mode, not to be confused with Power Down Mode. The sleep function must be enabled in every packet to continue in sleep mode. Set this bit to 0 to exit Sleep mode.

VAD:
In order to set the Voice Activity Detector on, set the VAD to 1. To turn the Voice Activity Detector off, set the VAD to 0.

5.2.10 Framed Input: Words 12-23 : Channel Data

This is the field that contains the actual coded bits. Input of the data begins with the MSB of the first word in this field and continues through with the final bit output being the LSB of the final word. If the data rate selected is less than 9600bps then the unused bits in each frame are zero and populate the end of the field. As is noted in the Channel Interface definitions, these unused bits must still be clocked out of the AMBE-2020™. The packet must always consist of 24 word

5.3 Framed Output Format

The format for framed output data is shown in Figure 5-B. Only the bits in the Channel data field are transmitted along with framing information (data used to locate the start of each frame for proper reconstruction at the decoder) over the channel. The first 192 bits provide overhead information which is sometimes useful to the host but is generally not transmitted over the channel.

Figure 5-B Basic Framed Output Format

20 ms frame	24 sixteen-bit words = 48 bytes = 384 bits	(12) 16 bit words of overhead (192 bits)	Word #	Description	
			0	Header always set to 0x13ec	
			1	Power Control ID (8bits)	Control Word 1 (8 bits) – see Table 5-J
			2	Rate info 0	
			3	Rate info 1	
			4	Rate info 2	
			5	Rate info 3	
			6	Rate info 4	
			7	Bit Error Rate	
			8	Soft Decision Distance	
			9	Detected Bit Errors In Current Frame	
			10	DTMF Control – see Table 5-L	
			11	Control Word 2 – see Table 5-N	
		(12) 16 bit words of data (192 bits)	12	Channel Data	
			13	Channel Data	
			14	Channel Data	
			15	Channel Data	
			16	Channel Data	
			17	Channel Data	
			18	Channel Data	
			19	Channel Data	
			20	Channel Data	
			21	Channel Data	
			22	Channel Data	
			23	Channel Data	

5.3.1 Framed Output: Word 0 : Header

The header is a 16 bit word that begins each valid frame corresponding to 20 milliseconds of speech. This field will always be **0x13EC**.

5.3.2 Framed Output: Word 1 : Power Control ID

The encoder will always use **0x00** in the 8-bit field of an output frame.

5.3.3 Framed Output: Word 1 : Control Word 1

This 8-bit control word indicates the activity of various functions.

Table 5-J Control Word 1 Format

Control Word 1 – 8-bits (See Table 1-A)							
7: MSB	6	5	4	3	2	1	0: LSB
Unused	Unused	**Decoder Frame Repeat**	**Decoder Silence Detect**	Unused	Unused	**Encoder Silence Detect**	**Encoder DTMF Detect**

Decoder Frame Repeat: When the Decoder Frame Repeat flag is set to 1, the decoder is reporting that the last frame decoded was a repeat of the previous frame.

Decoder Silence Detect: When the Decoder Silence Detect flag is set to 1, the decoder is reporting that the last frame decoded was a comfort noise frame.

Encoder DTMF Detect: The Encoder DTMF Detected Flag will be set to a 1 when the encoder detects a DTMF tone.

Encoder Silence Detect: The Encoder Silence Detected Flag will be set to 1 when no voice activity is detected. The Silence Detect option is controlled by and can be disabled by the VAD as described in section 5.2.9.

5.3.4 Framed Output: Words 2-6 : Rate Information

Rate Info 0, Rate Info 1, Rate Info 2, Rate Info 3, Rate Info 4.

Words 2-6 in the packet indicate the rate at which the AMBE-2020™ encoder is operating . These words are output. See tables 5-C and 5-D for corresponding values.

5.3.5 Framed Output: Word 7 : Bit Error Rate

This status field is used for the decoder to report bit error information. The 16 bit number output is used to compute the BER using the following calculation

$$\% \text{ BER} = (\text{Word } 7) / (32768) \times 100$$

This status field works in conjunction with the RIS bits in control word 2. Every time the RIS bits are set to any value other than 0x3, this field is reset. The BER is calculated only when using FEC provided by the AMBE-2020™.

5.3.6 Framed Output: Word 8 : Soft Decision Distance

This status field is used in conjunction with hardware pin 79 SOFT_EN. This field is used to report the soft decision distance for the most recent frame.

This status field works in conjunction with the RIS bits in control word 2. Every time the RIS bits are set to any value other than 0x3, this field is reset. The Soft decision Distance is calculated only when using Soft Decision decoding provided by the AMBE-2020™.

5.3.7 Framed Output: Word 9 : Detected Bit Errors

This status field is used to report the number of detected bit errors in the current frame.

This status field works in conjunction with the RIS bits in control word 2. Every time the RIS bits are set to any value other than 0x3, this field is reset. The number of bit errors is calculated only when using FEC provided by the AMBE-2020™.

5.3.8 Framed Output: Word 10 : DTMF Control

This word corresponds to the DTMF Detection capabilities of the vocoder. It uniquely identifies specific tones recognized by the encoder. See table 5-M for a list of tones and their corresponding values.

Table 5-K DTMF Tone Detection Parameters

DTMF Tone Detection Requirement	Value	Description
Minimum Input Level	-25 dBm0	An input signal shall not be rejected as a DTMF tone if its amplitude is greater than -25 dBm0 (maximum sinusoid dBm0 is defined as+3.17 dBm0).
Minimum Signal to Noise Distortion ratio	15 dB	In order for an input signal to correspond to a valid DTMF tone, the ratio of inband to out-of-band energy must be greater than 15dB. Inband energy is defined to be the energy in frequency components within ±3.5% of the two frequencies defined by the DTMF frequencies. Out-of-band energy is defined to be the total energy minus in the inband energy.
Minimum Frequency Tolerance	±1.5%	An input signal shall not be rejected as a DTMF tone if both of its principal frequency components are within ±1.5% of the frequencies needed for the DTMF tone.
Maximum Frequency Tolerance	±3.5%	An input signal shall be rejected as a DTMF tone if either of its principal frequency components are outside ±3.5% of the frequencies needed for the DTMF tone.
Normal Twist Range	8-10 dB	An input signal does not correspond to a valid DTMF tone if the energy contained within the low frequency band is more than 10 dB greater than the energy contained in the high frequency band. An input signal shall not be rejected as a DTMF if energy contained within the low frequency band is less than 8 dB greater than the energy contained in the high frequency band. Each low and high frequency band is limited to ±3.5% of the frequencies needed for the DTMF tone.
Reverse Twist Range	4-10 dB	An input signal does not correspond to a valid DTMF tone if the energy contained within the high frequency band is more than 10 dB greater than the energy contained in the low frequency band. An input signal shall not be rejected as a DTMF if energy contained within the high frequency band is less than 4 dB greater than the energy contained in the low frequency band. Each low and high frequency band is limited to ±3.5% of the frequencies needed for the DTMF tone.
Minimum Tone Duration	45 mS	An input signal shall not be rejected as a DTMF tone as long as its time duration is greater than 45 mS. In addition a minimum of two frames will be transmitted of the DTMF tone if a valid tone is detected. The duration of a tone is defined by the points at which the envelope is 20 dB below its peak value.

Table 5-L DTMF Control Format

DTMF Control – 8-bits (See Table 1-F)															
15: MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0: LSB
DTMF Amplitude								DTMF Digit Detect/ Generate							

Table 5-M DTMF Codes for Digit Detect/ Generate

DTMF Code	DTMF Digit	Frequency 1 (Hz)	Frequency 2 (Hz)
0x80	1	1209	697
0x84	2	1336	697
0x88	3	1477	697
0x81	4	1209	770
0x85	5	1336	770
0x89	6	1477	770
0x82	7	1209	852
0x86	8	1336	852
0x8A	9	1477	852
0x87	0	1336	941
0x83	*	1209	941
0x8B	#	1477	941
0x8C	A	1633	697
0x8D	B	1633	770
0x8E	C	1633	852
0x8F	D	1633	941
0xff	No Tone	N/A	N/A

If no tones are detected , the DTMF code is set to 0xFF. Dial, ring, and busy tones are standard North American call progress tones. An expanded list of tones and values can be found in the Appendices, Section 8.4.

DTMF Amplitude

The DTMF Amplitude runs from 3 to –60 dBm0. The value is a signed byte. So 0x03 = 3, 0x00 = 0, 0xff = -1, 0xc4 = -60.

5.3.9 Framed Output: Word 11: Control Word 2

Table 5-N Control Word 2 Format

Control Word 2 – 16															
Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Decoder Output Volume Control								Unused 0	Unused 0	Unused 0	Unused 0	SL	EE	RIS	

Rate Information Selector (RIS) :

This field is used to indicate which part of the device is affected by words 2-6, the rate control words.

Table 5-O Rate Information Selection Codes

value	Area Controlled
0x0	Encoder and Decoder
0x1	Encoder only
0x2	Decoder only
0x3	Neither Encoder nor Decoder

Encoder Enable (EE):
A value of 1 in the EE field of Framed output Word 11 Control Word 2 indicates that the Decoder was enabled and the Encoder did not run.

Sleep (SL):
A 1 in this field indicates the device has been put into sleep mode.

Decoder Output Volume Control: Indicates the current decoder volume.

5.3.10 Framed Output: Words 12-23 : Channel Data

This is the field that contains the actual coded bits. Output of the data begins with the MSB of the first word in this field and continues through with the final bit output being the LSB of the final word. If the data rate selected is less than 9600bps then the unused bits in each frame are zero and populate the end of the field. As is noted in the Channel Interface definitions, these unused bits must still be clocked out of the AMBE-2020™. The packet must always consist of 24 words.

5.4 Unframed Serial Format

The Unframed Format for the channel data is useful for applications which desire minimal glue logic between the AMBE-2020™ and the channel hardware. The use of minimal hardware in place of a microcontroller can be realized using this data format. Another distinct difference in this data format is that framing information (data which carries the positional information relating to the coded bits) is embedded into the data stream itself. Using this data format, the system designer need only transfer the coded data itself. A single bit from each frame is 'borrowed' from the voice data to embed the framing information. Keep in mind that this 'borrowed' bit reduces the effective voice coding rate quality by 50 bits per second. For example, a system with no FEC running at 2450 bps in Unframed mode will sound equivalent to one running at 2400 bps in Framed mode.

The designer should also be aware that it takes approximately 15 frames (300 milliseconds) for the decoder to attain synchronization with the incoming stream before it can output synthesized speech. Systems which are attempting to save power by shutting down transmission during periods of silence, and then resuming during periods of speech can not handle this 300 millisecond delay for each synchronization, and thus should use Framed mode with a more sophisticated framing method.

The 16 bit per word format, pictured in Section 5.2, is maintained in this mode but only a fraction of the full 16 bits is used to transfer the coded data. The user selects whether 1, 2, 3 or 4 bits will be transferred in each word based on pins BAUD_SEL[0:1] Table 4-B. **IMPORTANT:** The voice coding data rate selected must be evenly divisible by the number of voice data bits per word selected.

5.4.1 Unframed Serial Output Format

The Unframed output format contains 1 to 4 bits within each 16 bits serial output word. The formats which contain more than one bit each word the MSB of the data bits is considered first in the transmission. In Unframed mode, only the coded voice data bits are output. None of the superfluous information that exists in framed mode is available in this mode. The number of words that need to be transferred out of the encoder for each 20 millisecond frame will be the number of bits per frame divided by the number of bits per word. So a system coding at 4800 bps with 3 bits per word will need to read 32 ([4800 ÷50] ÷3 = 32) words each frame. The serial clock rate is computed by1/ [20 msec /(32 x 16)] = 25.6 kHz. If passive unframed mode is selected, the data strobe will be computed by 1/[20msec / 32] = 1.6 kHz.

Table 5-P Unframed Serial Output Data Format

Bits per Word See **Table 4-A**	Data				Unused											
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1 bit per Word Format	**D** msb	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2 bits per Word Format	**D** msb	**D**	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3 bits per Word Format	**D** msb	**D**	**D**	0	0	0	0	0	0	0	0	0	0	0	0	0
4 bits per Word Format	**D** msb	**D**	**D**	**D**	0	0	0	0	0	0	0	0	0	0	0	0

5.4.2 Unframed Serial Input Format

The Unframed Input format contains 1 to 4 bits within each 16 bits serial output word. For the formats which contain more than one bit each word the MSB of the data bits is considered first in the transmission. In Unframed mode, the header data from Framed mode is dropped and each 16 bit write contains 1 to 4 coded voice data bits. The number of words that need to be transferred into the decoder for each 20 millisecond frame will be the number of bits per frame divided by the number of bits per word. So a system coding at 4800 bps with 3 bits per word will need to write exactly 32 ([4800 ÷50] ÷3 = 32) words each frame.

Table 5-Q Unframed Serial Input Data Format

Bits per Word See **Table 4-A**	Data				Control Offset				Control Data							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1 bit per Word Format	**D** msb	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2 bits per Word Format	**D** msb	**D**	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3 bits per Word Format	**D** msb	**D**	**D**	0	0	0	0	0	0	0	0	0	0	0	0	0
4 bits per Word Format	**D** msb	**D**	**D**	**D**	0	0	0	0	0	0	0	0	0	0	0	0

6 A/D-D-A Interface

6.1 A/D-D/A Overview

The interface from the analog world of speech to the AMBE-2020™ is typically an A/D-D/A chip. Selection of the A/D-D/A chip should be made carefully, with a preference given to 16 bit linear devices. Additionally, consideration should be given for signal to noise ratios and filtering characteristics typically built into many such devices. Generally speaking, the flatter the frequency response over the voice spectrum (20-4000Hz) the better the overall system will sound.

The AMBE-2020™ Vocoder Chip operates with a speech data sample rate of 8kHz for both the A/D and D/A interfaces. This 8kHz data is input and output using a serial port on the AMBE-2020™.
In order to simplify the process of configuring the interface to the A/D-D/A chip, a number of preset configurations can be chosen through the CODEC_SEL[1-0] pins shown in Table 6-A. These preset configurations control companding and sampling rate as well as the sequence of programming words for the programmable devices, specifically the AD73311.

6.2 Configuring the A/D-D/A Interface using CODEC_SEL[1-0]

In order to simplify the process of configuring the A/D-D/A interface certain preset configurations are available to the user. Selection of these preset modes is made through the 2 hardware pins CODEC_SEL[1-0]. In Table 6-A, the 2 digit binary value for CODEC_SEL[1-0] corresponds to the levels present on the hardware pins, with a 0 corresponding to GND, and a 1 corresponding to VCC.

Table 6-A CODEC_SEL[1-0] : A/D-D/A Hardware Configuration Values

A/D-D/A Type	CODEC_SEL[1-0] pins 85,84
Generic 16 bit Linear 8Khz	00b
Analog Devices 73311 32kHz	01b
Generic μlaw 8kHz	10b
Generic Alaw 8kHz	11b

6.3 Low Level A/D–D/A Timing

Low Level Timing for A/D-D/A

Figure 6-A Low Level Timing for A/D-D/A

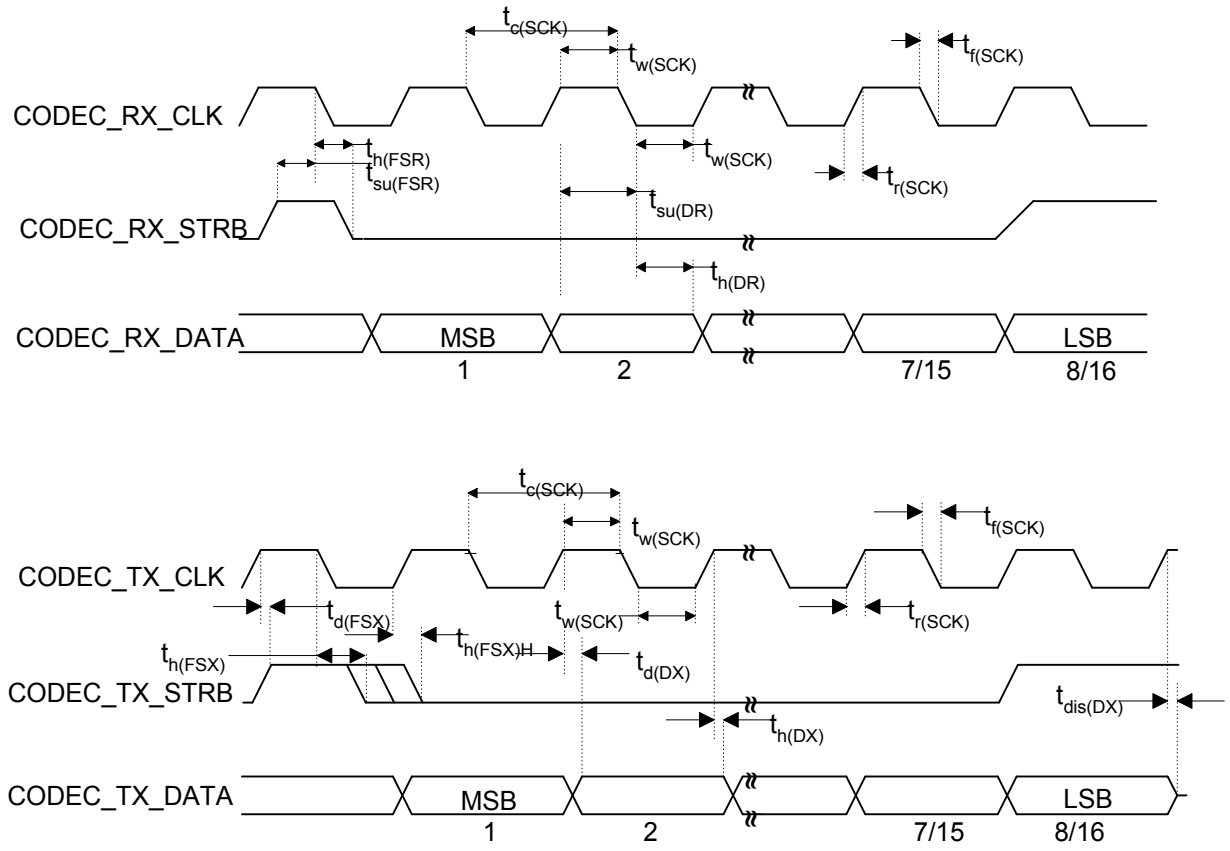


Table 6-B Switching Characteristics Over Recommended Operating Conditions for Serial Port Receive

Reference	Parameter	3.3 Volts		Units
		Min	Max	
$t_{h(FSR)}$	Hold time, FSR after CLKR falling edge	6		ns
$t_{h(DR)}$	Hold time, DR after CLKR falling edge	6		ns

Table 6-C Switching Characteristics Over Recommended Operating Conditions for Serial Port Receive

Reference	Parameter	3.3 Volts		Units
		Min	Max	
$t_{d(DX)}$	Delay time, DX valid after CLKX rising (Passive Mode)		25	ns
$t_{c(SCK)}$	Cycle time, serial port clock	6H		ns
$t_{f(SCK)}$	Fall time, serial port clock		6	ns
$t_{r(SCK)}$	Rise time, serial port clock		6	ns
$t_{w(SCK)}$	Pulse duration, serial port clock low/ high	3H		ns
$t_{su(FSR)}$	Setup time, FSR before CLKR falling edge	6		ns
$t_{su(DR)}$	Setup time, DR before CLKR falling edge	6		ns
$t_{d(FSX)}$	Delay time, CLKX rising to FSX		15	ns
$t_{d(DX)}$	Delay time, CLKX rising to DX (Active Mode)		15	ns
$t_{h(FSX)}$	Hold time, FSX after CLKX falling edge	6		ns
$t_{h(FSX)H}$	Hold time, FSX after CLKX rising edge		2H-5	ns
$t_{dis(DX)}$	Disable time, CLKX rising to DX		20	ns
$t_{h(DX)}$	Hold time, DX valid after CLKX rising edge	-5		ns

- Note: H = 7.629 ns; however, do not operate serial clocks any faster than 2.048 MHz. Thus $t_{c(SCK)}$ should be a minimum of 488.3 nsec.

7 Special Functions

7.1 Hardware vs. Software Selection Note

Many of the functions of the AMBE-2020™ can be accessed through both a hardware and software interfaces to the device. The following hardware inputs, CHANN_SEL[1-0], RATE_SEL[4-0], CODEC_SEL[1-0], VAD_EN, ENCODER_EN, and SLEEP_EN, are only accessed for input during the first 200 microseconds after a hardware reset on RESETN. For predictable operation these signals *must* remain stable over this time period. After this initialization period the functions that these pins access can only be reconfigured through the channel interface described in section 5.2. Changes on these pins after the 200 microseconds initialization period after reset are ignored, unless another reset is performed.

7.2 Coding Rate Selection

The Voice coding rate as well as the FEC coding rate can be selected individually on the AMBE-2020™. These rates are selected by using Rate Info words as described in section 5.2.4, or through hardware pins RATE_SEL[4-0] subject to the restrictions in section 7.1. The five input pins RATE_SEL[4-0] give 32 preconfigured voice/FEC rates. If rates other than these are desired then the Rate Info Words (in the Framed channel interface) can be used to configure voice and FEC rates in 50 bps increments.

Table 7-A Rate Selection Using Rate Info 0-4, compatible w/ AMBE-1000™ (AMBE™)

RATE_SEL4 Pin	RATE_SEL3 Pin	RATE_SEL2 Pin	RATE_SEL1 Pin	RATE_SEL0 Pin	Speech Rate (bps)	FEC Rate (bps)	Total Rate (bps)
0	0	0	0	0	2400	0	2400
0	0	1	0	1	2350	50	
0	0	0	0	1	3600	0	3600
0	1	0	1	1	3350	250	
0	1	1	1	1	4000	0	4000
0	1	1	1	0	3750	250	
0	0	0	1	1	4800	0	4800
0	0	1	1	1	4550	250	
0	0	0	1	0	3600	1200	
0	1	0	0	0	3100	1700	
0	1	0	1	0	4150	2250	6400
0	1	0	0	1	4400	2800	7200
0	1	1	0	0	7750	250	8000
0	1	1	0	1	4650	3350	
0	0	1	0	0	9600	0	9600
0	0	1	1	0	4850	4750	

Table 7-B Rate Selection Using Rate Info 0-4, AMBE-2020™ only (AMBE+™)*

RATE_SEL4 Pin	RATE_SEL3 Pin	RATE_SEL2 Pin	RATE_SEL1 Pin	RATE_SEL0 Pin	Speech Rate (bps)	FEC Rate (bps)	Total Rate (bps)
1	1	1	1	1	2000	0	2000
1	0	0	0	0	3600	0	3600
1	0	0	0	1	4000	0	4000
1	0	1	1	0	2400	1600	
1	0	0	1	0	4800	0	4800
1	1	0	0	0	4000	800	
1	0	1	1	1	3600	1200	
1	1	0	0	1	2400	2400	
1	0	0	1	1	6400	0	6400
1	1	0	1	0	4000	2400	
1	1	0	1	1	4400	2800	7200
1	0	1	0	0	8000	0	8000
1	1	1	0	0	4000	4000	
1	0	1	0	1	9600	0	9600
1	1	1	0	1	3600	6000	
1	1	1	1	0	2400	7200	

***Note: AMBE+ is only used for speech rates at 3600 bps and higher. Any rates below 3600 bps use a modified algorithm similar to the AMBE algorithm.**

7.3 Voice Activation Detection (VAD), Comfort Noise Insertion (CNI)

The Voice Activation Detection (VAD) algorithm along with the Comfort Noise Insertion (CNI) feature of the AMBE2020™ chip performs useful functions in systems trying to convert periods of silence, that exist in normal conversation, to savings in system bandwidth or power.

With the VAD functions enabled, periods of silence will be denoted by the encoder in two ways. First, the encoder will output a silence frame (in-band). This silence frame contains information regarding the level of background noise, which allows the corresponding decoder to synthesize a "Comfort Noise" signal at the other end. The comfort noise is intended to give the listener the feeling that the call is still connected, as opposed to producing absolute silence, which can give the impression that, the call has been "dropped". Second, the Encoder Silence Detected flag is set in Control Word 1 of the Framed Output format described in section 5.3.3.

VAD can be enabled in one of two ways. A logic high signal on the hardware pin VAD_EN (pin 86), subject to the restrictions of section 7.1, enables the VAD function. Once the AMBE2020™ has begun operating, control word 2 is used to enable/disable VAD as described in section 5.2.9.

If the VAD features are being used to reduce transmit power during times of conversational silence, DVSI recommends that a silence frame be transmitted at the start of the period and approximately each 500-1000 milliseconds thereafter. This is to ensure that the parameters regarding the levels of background noise are transmitted to the decoder for the smoothest audible transitions between synthesized speech and synthesized silence.

The silence threshold value is -25 dBm0 in the VAD algorithm. Each frame that exceeds this level will be classified as voice. If the frame level is less than –25 dBm0 the voice/silence decision will be determined based upon various adaptive thresholds.

The synthesis of a Comfort Noise frame by the decoder is *not* dependant on VAD being enabled. The decoder will produce a comfort noise frame if it receives an in-band silence frame (produced only by an encoder with VAD enabled).

7.4 Dual Tone Multiple Frequency, Detection and Generation

The AMBE-2020™ Vocoder Chip is capable of detecting, transmitting, and synthesizing DTMF tones. DTMF features are always enabled. Detection of a DTMF tone by the encoder sets the Encoder DTMF Detected Flag described in section 5.3.3. The DTMF tone detected along with amplitude information is placed in the DTMF Control Word as described in section 5.3.8. Additionally, the encoder passes the DTMF data in-band (within the regular voice data bits) so that normal DTMF tones pass seamlessly from the encoder to the decoder for synthesis.

The decoder synthesizes a DTMF tone in response to reception of an in-band DTMF tone frame or by setting the DTMF Control word as described in section 5.2.8.

7.5 Normal Power and Power Saving Modes

Power savings can be achieved during times of longer inactivity of the AMBE-2020™ chip by placing it into one of three available Low Power Modes. The chip can be placed into low-power and stand-by modes via hardware or software Control Words. In low power modes the A/D-D/A port will be disabled, concurrently halting any processing of voice frames in either direction. Depending on the low power state selected, either a Wake Up Control Word or a hardware reset on RESETN is necessary to return the AMBE-2020™ to normal operation.

7.5.1 Standard Sleep Mode

The standard sleep is the only low power mode that can be entered into either through hardware or software. The AMBE-2020™ Chip can be placed into Standard Sleep mode either by setting SLEEP_EN (pin 83) high, subject to the restrictions of section 7.1, or through software by using Control Word 2 with bit 3 set to 1 as described in section 5.2.9.

SLEEP_EN should be tied high if you plan to configure the A/D-D/A chip from Standard Sleep mode upon power-up or reset.

When using software SLEEP_EN with A-law or μ-law codecs, it is important to note that if packets are sent to the decoder while it is in sleep mode, noise will be heard at the output. It is recommended that no packets be sent to the decoder until it is commanded to wake up.

7.5.2 Power Down

Power Down provides the lowest power usage of the sleep modes, the only drawback to this mode is the necessity of a hardware reset on RESETN (pin 69) to resume normal operation.

Table 7-C Summary of Power Saving Modes

Sleep Mode	Enter State via	Return to Normal Operation via	Wake Up Time	Power Consumption	
				3V	
				Crystal	CMOS TTL
Normal Operation	N/A	N/A	N/A	Approx. 65mW	
Standard Sleep	SLEEP_EN pin at reset OR Control Word	Control Word	N/A	24 mW	36 mW
Power Down	Control Word	RESETN	95 ms.	**0.11 mW**	**0.11 mW**

7.6 Slip Enable

In any real time communication system, clock skew issues must be anticipated to keep the flow of data smooth from one end of the system to the other. The SLIP_EN (pin 82) signal allows the encoder of the AMBE-2020™ to react to small slips in the encoder channel signals. When the AMBE-2020™ is in active mode, the chip produces the signals internally for the transfer of data. Because this timing will then likely drive the transmission channel, the necessity of controlling slip becomes a moot point.

Any time the AMBE-2020™ encoder channel is in one of the passive modes and the channel timing is asynchronous to the A/D-D/A clock (very rarely are these two interfaces coupled) then the SLIP_EN pin should be set active high.

The AMBE-2020™ Vocoder chip process speech in voice frames that are approximately 20 ms in duration. When configured appropriately the chip provides a slip control feature that automatically adjusts the frame size to either 160 or 161 speech samples per frame. This slip control feature allows the vocoder chip to compensate for drift between the frame and sample rate clocks on the order of approximately 0.6% (6,000 ppm.) The vocoder chip also accepts Slip Control Packets that extend the range of allowable frame sizes to be between 159 and 161 samples per voice frame. When properly used these Slip Control Packets provide the designer with additional flexibility in dealing with clock drift.

There are three recommended methods for using slip control on the AMBE-2020™ Vocoder Chip which are described below. The system designer should select the method that best meets the needs of their system configuration. Also included is some background information on the operation of the AMBE-2020™ in passive mode

In order to help understand the Slip control feature here is a brief description on reading encoder packets from the AMBE-2020™ in passive framed mode.

When transmitting a packet, the AMBE-2020™ writes a Header = 0x13ec followed by 23 words of data, followed by 0xfffe into the transmit (i.e. output) buffer. The terminating word 0xfffe is written into the transmit buffer by the AMBE-2020™ at the end of each encoder packet. Normally in passive mode this terminating word is in the transmit buffer at the beginning of each transmission cycle (from the previous frame) and so it is the first word output whenever a packet is transmitted. If the encoder packet is ready, then the second output word will be the packet Header=0x13ec followed by 23 words of data. However if the packet is not ready then the AMBE-2020™ will continue to output the terminating word (0xfffe) until the packet is ready and placed in the transmit buffer. At this point the full 24 word packet beginning with the Header will be output on subsequent transmissions. This process continues for each packet transmission which occurs nominally every 20 ms, provided that each 24 word packet (Header + 23 data words) is read in full. If the full 24 words of the packet are not read from the AMBE-2020™, then the chip's transmit buffer will contain some words left over from a previous packet. Generally these words would be 0x0000 for lower data rates which don't use the last words of the packet. This case should be avoided hence:

It is recommended that in passive framed mode the system always read packets by requesting words from the AMBE-2020™ until a packet Header is received and then continuing to request 23 additional output words from the AMBE-2020™ until a total of 24 words beginning with the Header word = 0x13ec are received. Any words output by the AMBE-2020™ prior to the Header should be ignored by the system (except for monitoring as discussed in Method 3 below).

Word #	Value	Description
0	0x13ec	Header
1	0x07xx	Slip Control Packet ID, xx=CWD1 (See table 5-B) Typical value xx=00
2	0x12c9	Slip Control indicator for AMBE-2020™
3	0x009f	Slip Control data
4	0x0000	Must be 0x0000
5	0x0000	Must be 0x0000
6	0x0000	Must be 0x0000
7	0x0000	Must be 0x0000
8	0x0000	Must be 0x0000
9	0x0000	Must be 0x0000
10	0x0000	Must be 0x0000
11	0x0000	Must be 0x0000
12-23		Channel Data for AMBE® voice decoder

Table 7D: Slip Control Packet

Method 1 - Internal Slip Control

This is the simplest method of slip control and is the default method provided slip control is enabled (SLIP_EN is high) on the chip. In this method the vocoder chip's internal slip adjustment of 160 to 161 sample per frame is used. In order to work properly, the system designer must set-up the sample rate and packet timing so that the following constraint is met:

160 < Average-Frame-Interval * (1 +/- Frame-Drift) * Sample-Rate * (1 +/- Sample-Drift) < 161

For example using an Average-Frame-Interval = 20 ms, and assuming 100 parts per million oscillator accuracy (i.e Frame-Drift = Sample-Drift = .0001), then the above constraint requires:

8002 Hz < Sample-Rate < 8048 Hz.

In practice Sample-Rate=8002 Hz would be preferred since it is closer to the nominal value of 8000 Hz.

In another example the Sample-Rate = 8000 Hz. as provided by a PCM source. Again assuming 100 parts per million oscillator accuracy for both clocks (i.e. Frame-Drift = Sample-Drift = .0001), then the above constraint requires:

20.0041 ms. < Average-Frame–Interval < 20.1209 ms.

This can be achieved by slightly decreasing the channel bit rate or adding an extra bit into the channel bit stream every several voice frames.

Method 2 - Extended Slip Control with Periodic Slip Control Packets

The AMBE-2020™ can provide extended slip compensation through the insertion of Slip Control Packets. One method of using this capability is for the system to periodically insert these Slip Control Packets into the data stream sent to the AMBE-2020™. Note that for this method slip control must be enabled (SLIP_EN is high) on the chip. This approach gives the designer a way to accommodate clock drift while providing very flexible frame-interval and sample-rate timing. Furthermore minimal system overhead is required. In this method a Slip Control Packet is generated by the system by setting the Control Words as shown in Table 7D above, where the Channel Data is the compressed voice data being sent to the AMBE decoder. In the Periodic Slip Control method such a Slip Control Packet is input into the vocoder chip every N frames. The value of N must be selected by the design engineer to meet the following constraint:

0.25 > (1/N) > Average-Frame-Interval * Sample-Rate * (Frame-Drift + Sample-Drift)

For example with an Average-Frame-Interval = .02 (i.e. 20 ms) and a Sample-Rate = 8000, then with 100 parts per million oscillator accuracy (i.e. Frame-Drift = Sample-Drift = .0001), then above constraint equates to 4 < N < 31.25, and N=30 would be a reasonable selection. In this case the system would input the specified Slip Control Packet into the AMBE-20X0 vocoder chip every 30'th frame enabling the vocoder chip to adjust for the actual clock drift.

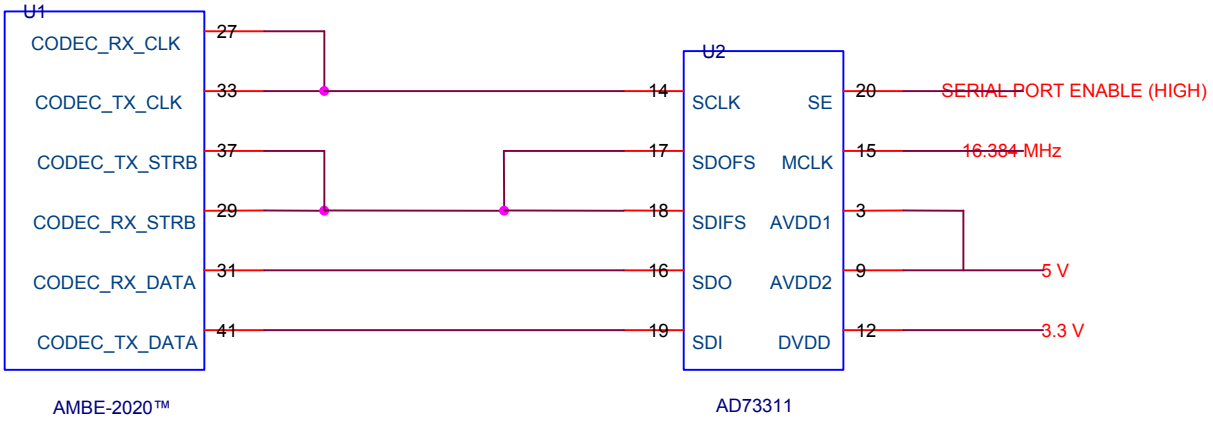
RECOMMENDED
Method 3 - Extended Slip Control with as needed Slip Control Packets

The preferred method for using Slip Control Packets is to monitor the availability of data from the AMBE-2020™ vocoder chip and to only input Slip Control Packets into the data stream sent to the AMBE-2020™ as needed. Note that for this method slip control must be enabled (SLIP_EN is high) on the chip. This method provides compensation for the widest range of clock drift (1.2% or 12000 ppm), with the greatest flexibility in frame-interval and sample-rate timing. In this method the same Slip Control Packets shown in Table 7D are inserted into the data stream going to the AMBE-2020™. However, unlike in the Periodic method, the packets are not input at regular intervals but are instead only input to the chip when needed. The recommended procedure for this Method of Slip Control is for the system to read a packet from the AMBE-2020™ at regular fixed frame intervals where the fixed interval must be within the range [19.875 – 20.125] ms for a sample rate = 8000 Hz. The system application should check each word output by the AMBE-2020™ and should continue requesting words from the chip until the packet Header followed by 23 data words are received. If the words received before the Header word consist of only a single termination word (0xfffe) then no further action is required. However if two or more termination words are received prior to the Header then the system should input a Slip Control Packet to the AMBE-2020™ on the next available transmission into the chip (i.e. the next packet going into the AMBE-2020™ decoder should be a Slip Control Packet). Once this Slip Control Packet is input into the AMBE-2020™ it will respond within 1-2 frames by advancing the time when packets are ready for transmission by 125 microseconds. Note that this procedure also may require a small amount of buffering in the system to account for the fact that the packet my not be ready for some small time (< 125 microseconds) after it is first requested.

8 Appendices

8.1 Example: AD73311 Usage

The following examples of A/D-D/A chips have been included to show connections necessary for interfacing to a number of popular chips.



REFERENCE DATA

The AMBE-2020™ sends the following configuration sequence to the AD73311 when CODEC_SEL[1-0]=01b:

0x8113, // write 13 to CRB of AD73311, MCD=1 (DMCLK=MCLK/2),SCD=0(SCLK=DMCLK/8)

0x82f9, // write f9 to CRC of AD73311, 5VEN, REFOUT, all Power ON

0x8300, // write 0 to CRD of AD73311

0x8001 // write 1 to CRA of AD73311 (Enters Data Mode)

8.2 Example: Texas Instruments TLV320AIC10 Usage

The Texas Instruments' TLV320AIC10 codec presents a simple low cost solution for use with DVSI's AMBE-2020™ vocoder chip. This application note provides information on interfacing these components. Figure 1 shows a sample block diagram interface, between the TLV320AIC10 codec and DVSI's AMBE-2020™ vocoder chip.

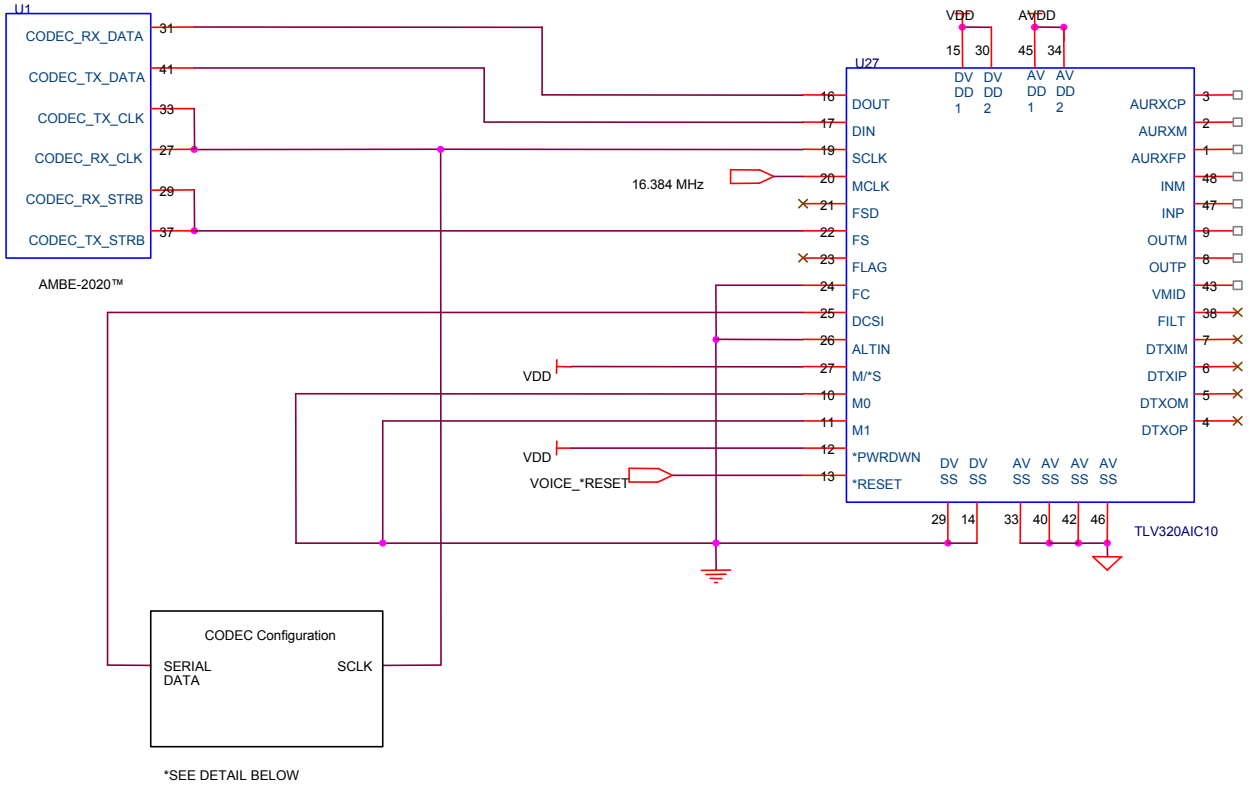


Figure 1: AMBE-2020™ and TLV320AIC10 sample block diagram

Configuration:

To configure the AMBE-2020™ for operation with the TLV320AIC10, set the CODEC_SEL pins on the AMBE-2020™ vocoder chip to work with a generic 16 bit linear 8 kHz codec as follows:
CODEC_SEL [1-0] (pins 85,84) = 00b

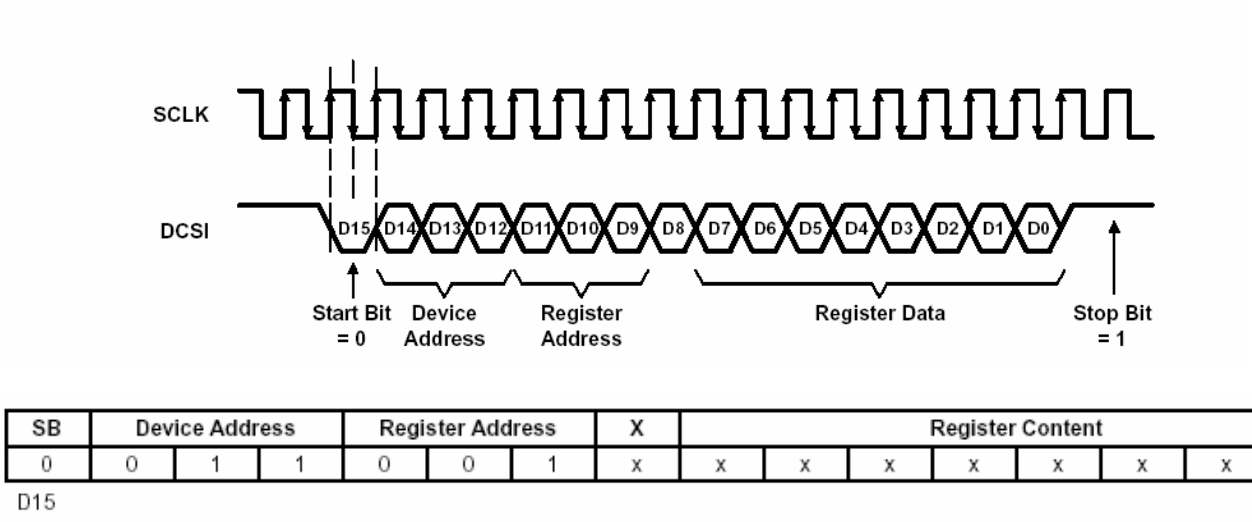
Initialization Procedure:

The control registers in the TLV320AIC10 codec must be initialized for proper operation. The recommended procedure is to initialize the TLV320AIC10 by writing data to its 4 control registers through the DCSI port, while the AMBE-2020™ is held in reset. The timing for the DCSI port is shown in Figure 2.

Note that the Device Address (D14-D12) is normally set to 0 unless multiple codec devices are used in cascade. Be sure that the stop bit is at least 2 clock pulses long between data words as shown in the timing diagram. Shift the control words into the device 1 bit at a time at the rate of SCLK.

Various configuration data can be used to control the operation of the TLV320AIC10 codec (see the data sheet for more information), however for reference the AMBE-2020™ has been tested with the TLV320AIC10 configured using the register values shown in Table 1. Once the TLV320AIC10 is configured, the AMBE-2020™ should be taken out of reset to begin communication with the codec.

The logic connected to the DCSI port does not have to be disabled. The user can make adjustments to the configuration as needed (for example ADC and DAC gain). A reset to the TLV320AIC10 codec will reset all of the internal registers. As a result, the TLV320AIC10 must be reconfigured following a reset.



SB	Device Address			Register Address			X	Register Content								
0	0	1	1	0	0	1	x	x	x	x	x	x	x	x	x	x
D15																D0

Figure 2: TLV320AIC10 configuration timing via DCSI port

Register Address (D11-D9)	**Configuration Data (D7-D0)**	**Notes:**
0x1	0x11	D4=1: select AUXP AND AUXM for ADC (Handset) D5=0: enable antialiasing filter D0=1: select 16 BIT data Format for DAC
0x2	0x08	D7=0: select normal Operation D4-D0=8: set Frequency Divider N=8
0x3	0x01	D7-D6=0: default operation D0=1: 16-Bit data format for ADC
0x4	0x00	D7-D4=0: ADC input gain = 0 dB D3-D0=0: DAC output gain = 0 dB Gain values can be adjusted as needed.

Table 1: Recommended TLV320AIC10 Configuration Data

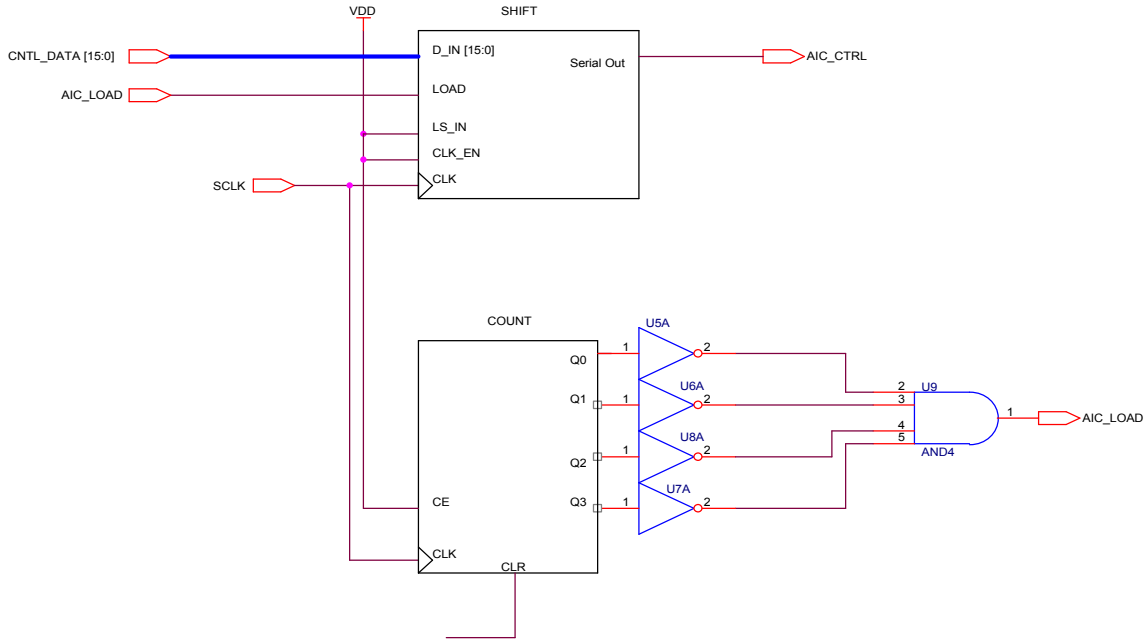
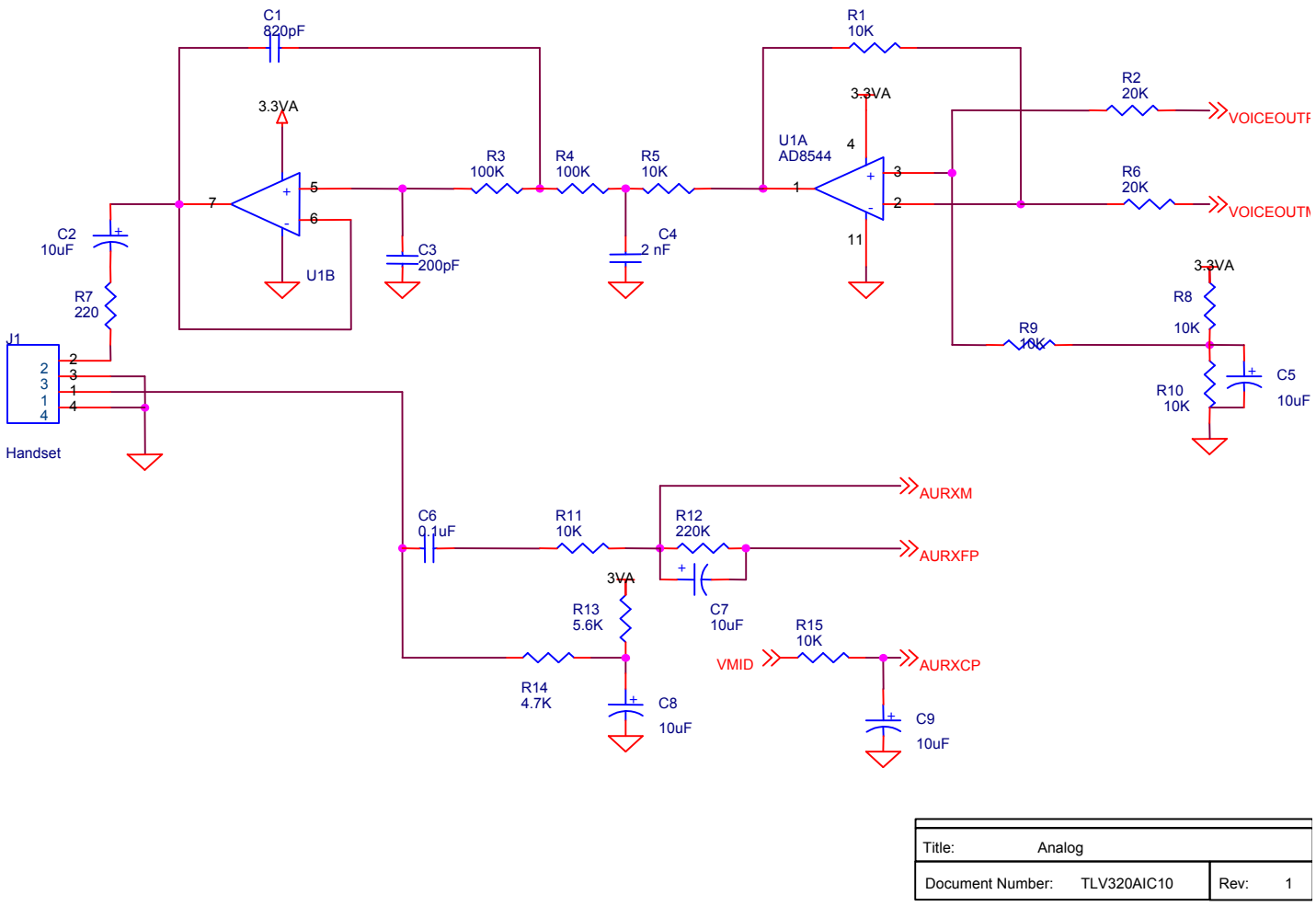


Figure 3: TLV320AIC10 Codec Configuration Detail

TLV320AIC10 Reference Schematic (Analog Section)



Reference Materials:

AMBE2020™ Vocoder chips Users Manual:
http://www.dvsinc.com/literature.htm

TLV320AIC10 Data Sheet:
http://www-s.ti.com/sc/ds/tlv320aic10.pdf

TLV320AIC10 EVM User's Guide:
http://www-s.ti.com/sc/psheets/slwu003d/slwu003d.pdf

Application Report – Understanding Data Converters:
http://www-s.ti.com/sc/psheets/slaa013/slaa013.pdf

8.3 Configuring the AD73311 for 3-Volt Operation

The Analog Devices AD73311 codec chip presents a simple low cost solution for use with DVSI's AMBE-2020™ Vocoder chip. This application note provides information on alternative methods of interfacing these components.

AD73311AR codec (using a 3 volt supply)
It may be desirable for the AD73311 AD/DA converter to be configured for a 3-volt supply voltage instead of a 5-volt supply voltage. The diagram and configuration procedure below outline the details necessary in order to send alternate configuration words to the CODEC.

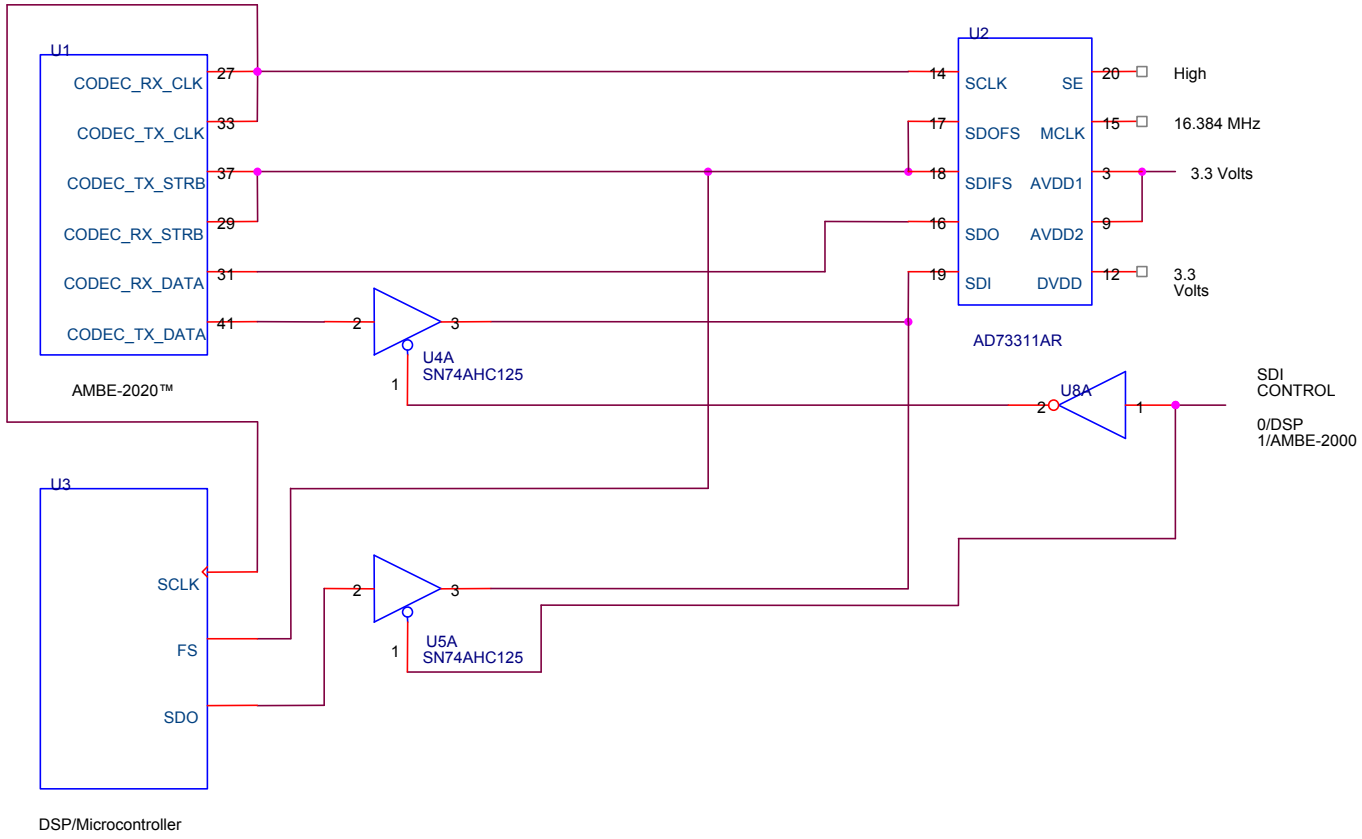


Figure 2: The AMBE-2020™ with the AD73311 Configured for 3-volt operation.

The objective of this circuit is to tri-state the output of the AMBE-2020™ CODEC_TX_DATA. This allows the DSP or Microcontroller to communicate with the AD73311 to send it the desired configuration.

Configure the AMBE-2020™ for operation with the AD73311 Codec. Set the CODEC_SEL pins as shown.
CODEC_SEL [1-0] (pins 85,84) = 01,b

Hold the CODEC_TX_DATA lines on the AMBE2020 in tri-state (in the circuit set the SDI bit to 0,b) during power up.

While the AMBE-2020™ lines are in tri-state, send the desired configuration words from the DSP/Microcontroller/logic to the AD73311 (Reset timing constraints for the AD73311 must be met).

After sending the configuration words set the SDI Control bit to 1,b (SEE NOTE). This sets the CODEC SDI line for normal operation with the AMBE-2020™.

NOTE: The SDI Control bit must be set to 0 for approximately 365 msec following a hardware reset.

Register Address (D10-D8)	Configuration Data (D7-D0)	Notes:
CRB 0x1	0x13	MCD = 1 Sets DMCLK=MCLK/2 SCD = 0 Sets SCLK=DMCLK/8
CRC 0x2	0x79	D6 = 1 Reference Out Enabled D5 = 1 Reference Power On D4 = 1 DAC Power On D3 = 1 ADC Power On D0 = 1 Power On
CRD 0x3	0x00	Gain set to 0
CRA 0x0	0x01	D0 = 1 Puts CODEC in Data Mode

Table 2: Alternate Configuration Data for the AD73311

AD73311L codec (3 volt supply)

The Analog Devices AD73311L is a low power 3 volt version of the AD73311. It is possible to use this part with the AMBE-2000™ or AMBE-2020™ vocoder chip utilizing the method described above for sending alternate configuration words to the AD73311 CODEC. Table 3 lists alternate control words for configuring the AD73311L for use with the AMBE-2000™ or AMBE-2020™.

Register Address (D10-D8)	Configuration Data (D7-D0)	Notes:
CRB 0x1	0x13	MCD = 1 Sets DMCLK=MCLK/2 SCD = 0 Sets SCLK=DMCLK/8
CRC 0x2	0x79	D6 = 1 Reference Out Enabled D5 = 1 Reference Power On D4 = 1 DAC Power On D3 = 1 ADC Power On D0 = 1 Power On
CRD 0x3	0x00	Gain set to 0
CRA 0x0	0x01	D0 = 1 Puts CODEC in Data Mode

Table 3: Configuration Data for the AD73311L

Additional Reference Material

AMBE-2020™ vocoder chip Users Manual
http://www.dvsinc.com/literature.htm

Application Report – Understanding Data Converters:
http://www-s.ti.com/sc/psheets/slaa013/slaa013.pdf

AD73311 - Data Sheet
http://www.analog.com/productSelection/pdf/AD73311_b.pdf

AD73311L - Data Sheet
http://www.analog.com/productSelection/pdf/AD73311L_a.pdf

8.4 Interfacing to the Texas Instruments PCM3500 Codec

The Texas Instruments PCM3500 codec chip presents a simple low cost solution for use with DVSI's AMBE-2000™ or AMBE-2020™ vocoder chips. This application note provides information on alternative methods of interfacing these components.

PCM3500

The block diagram in Figure 1 shows a sample interface between the PCM3500 codec and DVSI's AMBE-2000™ vocoder chip. The AMBE-2000™ or AMBE-2020™ CODEC_SEL bits (see AMBE-2000™ or AMBE-2020™ users manual) must be set for use with a generic 16 bit linear codec (CODEC_SEL1,0 – 00).

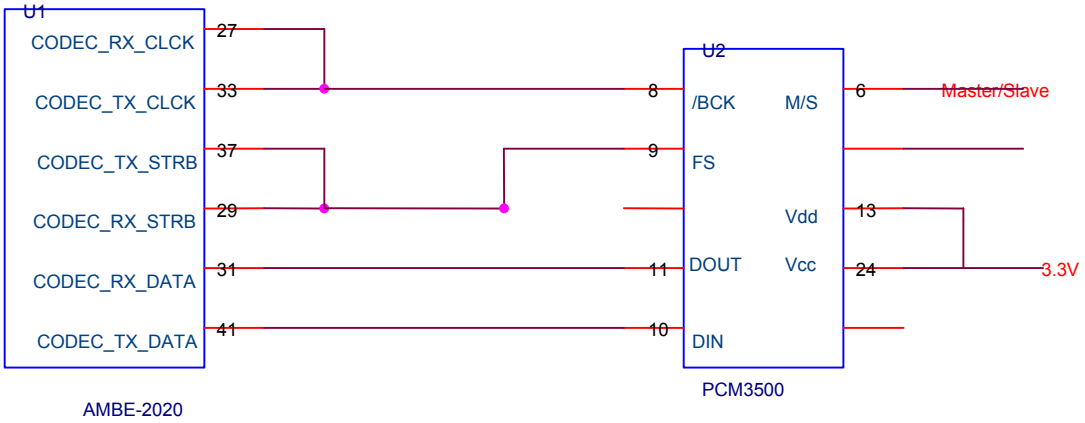


Figure 1: The AMBE-2020™ Vocoder with the PCM3500 CODEC

There are two advantages to using the PCM3500 codec. The first is the single supply design. The PCM3500 supports a single power supply design from +2.7 v to +3.6 v. The second advantage lies in its simplicity. There are no complicated configuration schemes associated with the codec. For configuration information, please see the PCM3500 data sheet and the reference circuit in Figure 2.

Notes On Analog Circuit Design

The example circuit assumes that a telephone handset is going to be used in the circuit. Typically, handset microphones have a very small gain and the output is at moderately low levels (on the order of 50 millivolts peak to peak). The PCM3500 Voice Codec is designed for an analog input voltage of 2 volts peak to peak. The analog input in the reference design is amplified (Gain = 22) in order to bring the handset voltage to the level expected by the ADC.

The output section is designed using a low pass filter design with a gain of 1. The filter is designed to allow the maximum amount of the voice signal to pass unimpeded. The output of the PCM3500 should be filtered for maximum voice quality.

Capacitors C13 and C14 are for creating a very low noise DC bias signal. If a low noise DC bias is available elsewhere in the circuit, they are not needed.

For optimum performance, the analog circuit should be adjusted for whatever input (and output) device is used. Please reference the PCM3500 data sheet for the analog requirements.

Application Information

It is strongly recommended that the user review the Application Information provided in the Texas Instruments PCM3500 data sheet before finalizing any design.

Additional Reference Material

AMBE-2000™ or AMBE-2020™ vocoder chip Users Manual
http://www.dvsinc.com/literature.htm

Application Report – Understanding Data Converters:
http://www-s.ti.com/sc/psheets/slaa013/slaa013.pdf

PCM3500 Data Sheet
http://www-s.ti.com/sc/ds/pcm3500.pdf

PCM3500 Evaluation Board
http://www-s.ti.com/sc/psheets/sbau028/sbau028.pdf

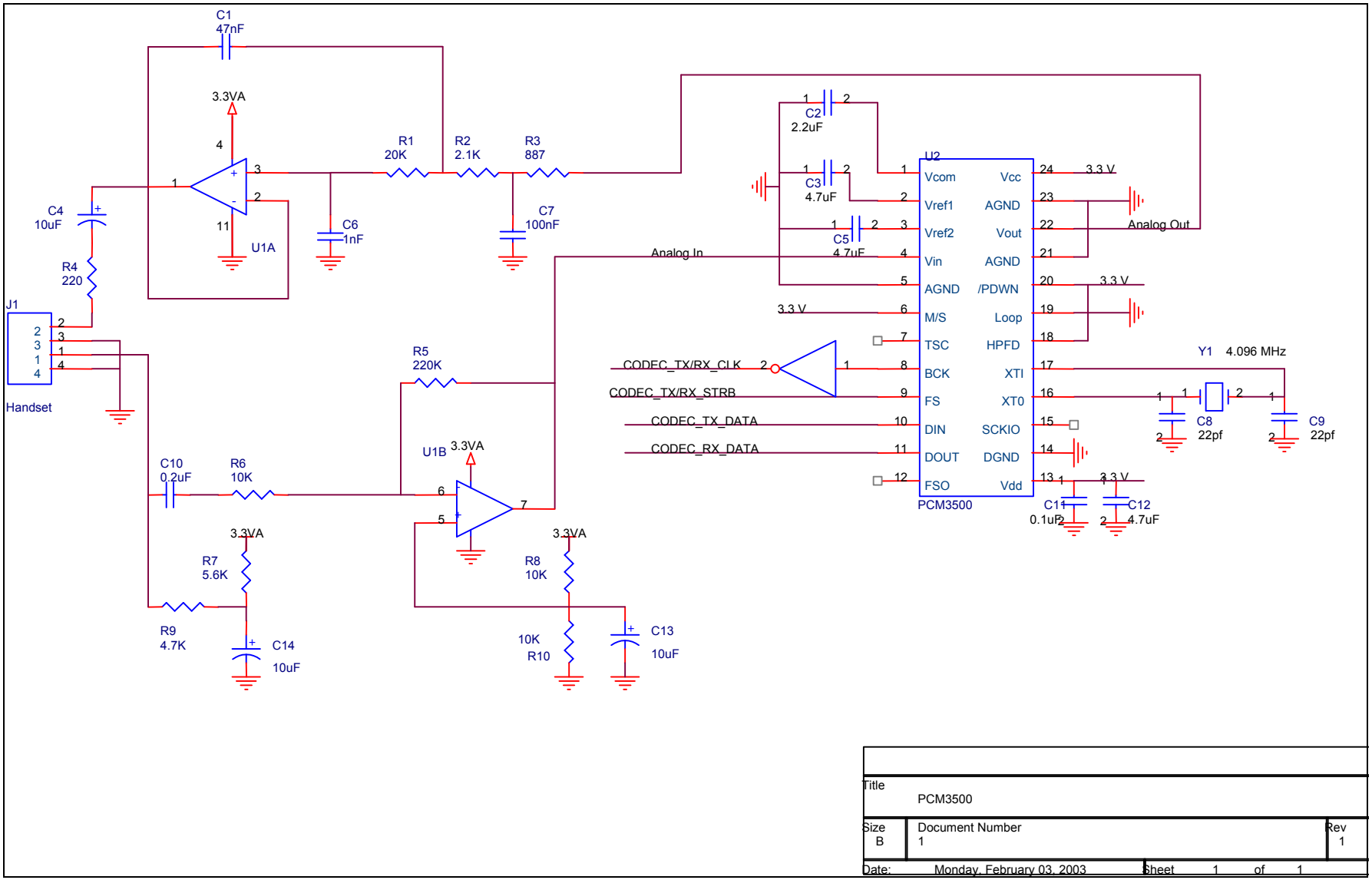

C1
47nF
3.3VA
R1
20K
R2
2.1K
R3
887
C2
2.2uF
C3
4.7uF
C5
4.7uF
U2
Vcom
Vref1
Vref2
Vin
AGND
M/S
TSC
BCK
FS
DIN
DOUT
FSO
Vcc
AGND
Vout
AGND
/PDWN
Loop
HPFD
XTI
XT0
SCKIO
DGND
Vdd
PCM3500
3.3 V
Analog Out
Analog In
C4
10uF
R4
220
J1
Handset
C6
1nF
C7
100nF
U1A
R5
220K
CODEC_TX/RX_CLK
CODEC_TX/RX_STRB
CODEC_TX_DATA
CODEC_RX_DATA
Y1
4.096 MHz
C8
22pf
C9
22pf
C10
0.2uF
R6
10K
U1B
R7
5.6K
R8
10K
R9
4.7K
C14
10uF
10K
R10
C13
10uF
C11
0.1uF
C12
4.7uF
Title
PCM3500
Size
B
Document Number
1
Rev
1
Date:
Monday, February 03, 2003
Sheet
1
of
1

Figure 2

8.5 Expanded Tone Detection and Generation

The AMBE-2000™ is capable of detecting and generating single tones as well as dual tones. The single tones span from 156.25 Hz to 3812.5 Hz in 31.25 Hz steps.

Tone Index (Decimal)	Tone Type	Freq #2 (Hz)	Freq #1 (Hz)
0-4	Invalid	N/A	N/A
5	Single	N/A	156.25
6	Single	N/A	187.5
7	Single	N/A	218.75
……	…….	……	……
122	Single	N/A	3812.5
123-127	Invalid	N/A	N/A
128	DTMF “1”	1209	697
…….	……..	…….	……
143	DTMF “D”	1633	941
144	Call Progress	440	350
145	Call Progress	480	440
146	Call Progress	620	480
147-254	Invalid	N/A	N/A
255	No Tone	N/A	N/A

8.6 Soft Decision Decoding

In modern communication systems the transmitter transmits information in the form of symbols. The demodulator takes the received signal and tries to decide which symbol was transmitted. In other words, the demodulator is making a decision based on the received signal. For instance, in a binary system, the symbols could be represented by a 1 and a 0. Because of interference and many other factors, these signals can be misinterpreted because of channel degradation. Significant improvement in FEC performance can be added by setting up the receiver so that the demodulator is making a finer estimation of the received energy prior to the decoder, this is called soft-decision decoding. The link below describes this in more detail.

http://www.mathworks.com/access/helpdesk/help/toolbox/commblks/usersguide/tutor135.shtml

The AMBE-2000/2020 utilizes a 4 bit soft decision decoder. The bits are defined as follows:

Decision Value (Binary)	**Interpretation**
0000	Most confident **0**
0111	Least confident **0**
1000	Least confident **1**
1111	Most confident **1**

Placing a logic high on pin 79 of either the AMBE-2000™ or AMBE-2020™ vocoder chips enables the soft decision error correction on the decoder. Enabling the soft-decision does nothing to the encoder packet. The packet will look like a normal encoded packet. The user must implement circuitry at the receive end of the channel for making a finer (4 bit) estimation of the received energy (see above link for an explanation of how this can be done).

The AMBE-2000/2020 decoder packet structure is altered. The decoder expects each voice data bit of the encoded packet to be represented by 4 soft decision (SD) bits. The decoder will make the decision of whether or not a 1 or a 0 is represented by the SD bits. Table 1 is an example of a soft-decision decoder packet.

Table 1. Soft-Decision Decoder Packet

20 ms frame	60 sixteen-bit words = 120 bytes = 960 bits		Word #	Description			
		(12) 16 bit words of overhead (192 bits)	0	Header always set to 0x13EC			
			1	Power Control (8 bits)		Control Word 1 (8 bits)	
			2	Rate info 0			
			3	Rate info 1			
			4	Rate info 2			
			5	Rate info 3			
			6	Rate info 4			
			7	Unused in Input			
			8	Unused in Input			
			9	Unused in Input			
			10	DTMF Control			
			11	Control Word 2			
		SD = 4 bits x 4 per word = 16 bit words of data x 48 words = 768 bits	12	SD0	SD1	SD2	SD3
			13	SD4	SD5	SD6	SD7
			14	SD8	SD9	SD10	SD11
			15	SD12	SD13	SD14	SD15
			16	SD16	SD17	SD18	SD19
			17	SD20	SD21	SD22	SD23
			18	SD24	SD25	SD26	SD27
			19	SD28	SD29	SD30	SD31
			20	SD32	SD33	SD34	SD35
			21	SD36	SD37	SD38	SD39
			22	SD40	SD41	SD42	SD43
			23	SD44	SD45	SD46	SD47
			24	SD48	SD49	SD50	SD51
			25	SD52	SD53	SD54	SD55
			26	SD56	SD57	SD58	SD59
			27	SD60	SD61	SD62	SD63
			28	SD64	SD65	SD66	SD67
			29	SD68	SD69	SD70	SD71
			30	SD72	SD73	SD74	SD75
			31	SD76	SD77	SD78	SD79
			32	SD80	SD81	SD82	SD33
			33	SD84	SD85	SD86	SD87
			34	SD88	SD89	SD90	SD91
			35	SD92	SD93	SD44	SD95
			36	SD96	SD97	SD98	SD99
			37	SD100	SD101	SD102	SD103
			38	SD104	SD105	SD106	SD107
			39	SD108	SD109	SD110	SD111
			40	SD112	SD113	SD114	SD115
			41	SD116	SD117	SD118	SD119
			42	SD120	SD121	SD122	SD123
			43	SD124	SD125	SD126	SD127
			44	SD128	SD129	SD130	SD131
			45	Sd132	SD133	SD134	SD135
			46	SD136	SD137	SD138	SD139
			47	SD140	SD141	SD142	SD143
			48	SD144	SD145	SD146	SD147
			49	SD148	SD149	SD150	SD151
			50	SD152	SD153	SD154	SD155
			51	SD156	SD157	SD158	SD159
			52	SD160	SD161	SD162	SD163
			53	SD164	SD165	SD166	SD167
			54	SD168	SD169	SD170	SD171
			55	SD172	SD173	SD174	SD175
			56	SD176	SD177	SD178	Sd179
			57	SD180	SD181	SD182	SD183
			58	SD184	SD185	SD186	SD187
			59	SD188	SD189	SD190	SD191

8.7 Special Rate 2350 bps Voice / 50 bps FEC AMBE-1000™ Vocoder Chip Compatible Mode

The following procedure is for implementing the AMBE-2000/2020™ in a special mode that is compatible to AMBE-1000™ Vocoder Chip at 2350 bps voice and 50 bps FEC.

This procedure is ONLY required when interoperating with the AMBE-1000™ Vocoder Chip at this specific rate (2350 voice + 50 bps FEC). All other rate configurations function as described in the AMBE-2000/2020™ Vocoder Chip Manual.

When implementing this compatible mode on the AMBE-2000/2020™ Vocoder Chip if the data rate is fixed and does not change, it is recommended to set the rate via the Rate_Sel configuration pins (Pins 74, 73 72, 71, 70) as shown in Table 1. By hardwiring these pins the procedure outlined below can be avoided.

AMBE-2000/2020™ Rate Selection Using Hardwired Rate Info 0-4, compatible w/ AMBE-1000™							
RATE_SEL4 **Pin 74**	RATE_SEL3 **Pin 73**	RATE_SEL2 **Pin 72**	RATE_SEL1 **Pin 71**	RATE_SEL0 **Pin 70**	Speech Rate (bps)	FEC Rate (bps)	Total Rate (bps)
0	0	1	0	1	2350	50	2400

Table 1.

Compatible Mode Procedure Step 1.

To enable the AMBE-2000/2020™ to interoperate with the AMBE-1000™ Vocoder Chip at the rate of 2350 bps voice + 50 bps FEC, first send the packet described in Table 2.

First Packet		
Word #	**Value**	**Description**
0	0x13ec	Header
1	0x0002	Power Control ID/Control Word 1
2	0x902f	Rate 0
3	0x0000	Rate 1
4	0x0000	Rate 2
5	0x0000	Rate 3
6	0x6930	Rate 4
7	0x0000	Unused
8	0x0000	Unused
9	0x0000	Unused
10	0x0000	DTMF Control
11	0x0000	Control Word 2
12-23		Channel Data for AMBE® voice decoder

Table 2.

Compatible Mode Procedure Step 2.

The next packet should be identical to the packet described in Table 3.

Special Control Packet		
Word #	**Value**	**Description**
0	0x13ec	Header
1	0x0700	Special Control packet
2	0x0834	Special control data
3	0x0005	Special control data
4	0x11bf	Special control data
5	0x0005	Special control data
6	0x0000	Must be 0x0000
7	0x0000	Must be 0x0000
8	0x0000	Must be 0x0000
9	0x0000	Must be 0x0000
10	0x0000	Must be 0x0000
11	0x0000	Must be 0x0000
12-23		Channel Data for AMBE® voice decoder

Table 3.

Compatible Mode Procedure Step 3.

After the packets detailed in Table 2 and Table 3 are sent into the AMBE-2000/2020™ Vocoder Chip the RIS bits in Control Word 2 must be set to 0x3 for each subsequent packet. If the rate is changed or the device is reset, the above procedure (steps 1, 2 and 3) must be repeated.

Control Word 2 – (16-bits)															
Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Decoder Output Volume Control								Unused 0	Unused 0	VAD	Unused 0	SL	EC	RIS	

Table 4.

History of Revisions

Revision Number	Date of Revision	Description	Pages
1.0	November 1999	Initial Version	
1.1	April 2000	Pin descriptions	11-12
		Serial Configuration Selection	19
		Channel Serial Interface Pin Descriptions	20
		Table 6-A CODEC_SEL[1-0]: A/D- D/A Hardware Configuration Values	35
1.2	August	Added AD73311 to AMBE-2020™ connection diagram	42
1.3	October	Pin Description : ENCODER_EN is pin 24.	11
		Corrections of Table 4A and 4B	19
		Clarification on VAD	28
		Expanded description of Control Word 1	30
		Table 5-M added DTMF Code 0xff	32
		Channel and Codec Timing Diagrams and Tables	21, 22, 36, 37
1.4	November 2000	Table 4B Corrected (pin 80 and 81)	19
		Added Note describing H	22, 37
2.0	January 2001	Clarified/corrected the following pages.	10, 11, 12, 13, 16, 17, 21, 22, 23, 27, 28, 29, 32, 34, 36, 37, 39
2.1	February 2001	Updated Timing Diagrams and Tables for Channel and Codec	21, 22, 36, 37
2.2	February 2001	Changed Pin Description CLK_I to X2/CLKIN and CLK_I2 to X1	11
		Updated timing diagram and table for X2/CLKIN and RESETN	13, 14
		Replaced …set the DTMF Code to 0x00 to …set the DTMF Code to 0xff	27
3.0	August 2001	Updated company address	2
		Removed description of Decoder Output Volume Control	28
		Modified SLEEP_EN Section 7.5.1	40
		Modified description of EPR	11, 12, 20
		Added Detailed Explination of Slip Enable Control	42, 43
		Added description of Decoder Silence Detect, Decoder Frame Repeat and Encoder DTMF Detect bits	30
4.0	January 2003	Various grammer changes	43
		Vad Threshold Explination	41
		Associated Delay	14
		Front End Requirements	9
		Added AD73311AR Configuration Words	46
		Added Tech Note 8.2	47
		Expanded DTMF Tone Chart	30, 34
4.1	April 2004	Added additional rate control words in Table 5-D	29
4.2	June 2004	Added tech note to Appendices section 8.7	60
4.3	February 2005	Added Decoder output volume control description section 5.2.9 Removed blank section 5.2.10	31
4.4	April 2005	Added Figure 3-G and text to section 3.6	20

History of Revisions			
Revision Number	**Date of Revision**	**Description**	**Pages**
4.5	Sept. 2006	Added Note 2 in Section 3.2	15
4.6	Dec. 06	Revised High-level input voltage, I/O values in Table 3e	21
4.7	May 07	Added Table 3G Section 3.10 Thermal Resistance Characteristics	22
4.8	Sept 07	Edited Table in Note 2 on page 15	15
4.9	Feb, 08	Edited Encoder Enable Description	37